Perancangan demodulator QPSK untuk perangkat modem power line communication (PLC) dengan menggunakan rangkaian logika = QPSK demodulator design for power line communication (PLC) modem based on discrete digital TTL circuit

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Abstrak

Skripsi ini dibuat untuk merancang demodulator QPSK untuk perangkat modem power line communication yang disusun dari rangkaian logika dengan menggunakan simulator Multisim 10. Rangkaian demodulator QPSK tersebut terdiri atas beberapa modul, seperti rangkaian sinusoidal to square wave, clock recovery, phase shifter, comparator, dan sampling. Keseluruhan modul rangkaian tersebut disimulasikan dengan menggunakan perangkat lunak Multisim 10. Proses pertama yang dilakukan di dalam rangkaian demodulator ialah mengubah modulated signal QPSK analog dari pre-amp receiver menjadi berbentuk pulsa (square wave). Proses berikutnya ialah mensinkronkan clock generator pada bagian demodulator dengan sinkronisasi clock yang dikirim oleh far end modulator dengan menggunakan rangkaian clock recovery. Rangkaian dasar QPSK adalah phase shifter, yang berfungsi untuk membangkitkan sinyal carrier dan menggeser fase sinyal sebesar 900. Modulated sinyal QPSK tersebut dibandingkan dengan sinyal carrier dengan rangkaian comparator. Proses terakhir ialah menggabungkan sinyal dari kanal I dan Q menjadi data serial, dengan menggunakan rangkaian sampling. Selanjutnya dilakukan analisis untuk menunjukkan cara kerja dari rangkaian demodulator QPSK ini, kestabilan rangkaian, hasil keluaran dari setiap proses rangkaian, dan hasil data QPSK yang dapat didemodulasikan menjadi data awal.
<hr>This paper explains the design of QPSK demodulator which is proposed for communication via power line networks. As already known that communication via power-line network needs suitable modulation, since power-line networks are very noisy and originally were not designed for communication. The QPSK modulation technique had been chosen, since it is one of the effective modulation methods to be implemented in the high noisy communication channel such as power-line networks. QPSK modulation is a well-known modulation technique in telecommunication field. One makes design different from existing design is the use of the electronic discrete components. In this research, it is shown that QPSK demodulator can be built up from discrete digital TTL integrated circuits which are enormously available in the market. This QPSK demodulator was designed by using simulation software called Multisim 10 Simulator. The QPSK demodulator consists of several blocks functions, such as sinusoidal to square-wave converter, phase shifter, clock recovery, clock generator, comparator and sampling circuit. This QPSK demodulator is designed to work in 250 KHz carrier frequency and having speed of about 60 kbps. Analysis has been made based on how the circuit works and comparison to the existing standard. This designed QPSK demodulator is concluded to be able to work and support for PLC system and in the future can be improved to obtain a better PLC modem performance.