A 2.3/3.3-GHz. Dual band low noise amplifier for WiMAX applications in Indonesia

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Abstrak

ABSTRAK
To support the WiMAX infrastructure development in Indonesiaa dualband 2.3/3.3 GHz low noise amplifier (LNA) is designed and analyzed. The LNA is designed by combining the inductive source degeneration architecture and the proposed switchable inductor for controlling gain. The chipis implemented by TSMC 0.18-μm CMOS technology.
First of all, the mathematical analysis of the proposed LNA architecture is conducted. It includesinput-impedance, gain and noise figure analysis. The proposed input-impedance analysis modifies the input impedance of the inductive source degeneration LNA architecture, includes devices selection to fulfill S11 requirement. Furthermore, the gain analysis is performed to explain the proposed switchable inductor structure for controlling gain. It shows that combining onchip inductor paralleled with series bond-wire and on-board inductor will obtain a flatter gain for two bands of interest. The noise figure for source inductive degeneration LNA architecture is derived. The noise figure described by the derived equations agrees well with that obtained from the simulation.
Secondly, the proposed dual-band 2.3/3.3 GHz LNA is simulated. At lowband mode, simulated results show the maximum S21 of 18.69 dB, an S11 below -29 dB, and a flat noise figure of 2.3 ~ 2.33 dB from 2.3 to 2.4 GHz. The LNA presents the IIP3 and the P1dB of -12.1 dBm and -23.3 dBm, respectively, while consuming 18.4 mW at 1.5 V power supply. At high-band mode, the simulation results show the S21 of 17.01 ~ 17.48 dB, the S11 below -21 dB, and an flat noise figure of 2.36 ~ 2.37 dB from 3.3 to 3.4 GHz. The LNA consumes only 12.9 mW at high-band mode, while exhibiting the IIP3 and the P1dB of -11.3 dBm and -22.1 dBm, respectively.
And then, the proposed LNA is verified by the post-simulation in which the bond-wire effects are considered for an on-board deployment. At low-band mode, the post-simulation results show the S11 of -29.11 dB ~ -32 dB, the S21 of 17.18 ~ 17.42 dB, and the flat noise figure of 2.67 ~ 2.71 dB. The LNA exhibits the IIP3 and P1dB of -13.4 dBm and -24.2 dBm respectively, while consuming 16.32 mW power. At high-band mode, the LNA exhibits the S21 of 15.5 ~ 15.88 dB, the S11 of -12.94 ~ -16.82 dB, and the flat noise figure of 2.52 ~ 2.54 dB while consuming 11.75 mW. The IIP3 and P1dB for the high-band mode are -12.3 dBm and 23.3 dBm, respectively. The total chip area ofthe proposed LNA is 0.9 mm2,

including the IO pads.