Perancangan VLSI 0.25 μm dengan desain hybrid VHDL berbasis FPGA Xilinx Spartan 3 untuk CPU ocean bottom unit Tsunami Early Warning System = VLSI design 0.25 μm of a hybrid design with VHDL Xilinx Spartan 3 FPGA-based for ocean bottom unit CPU Tsunami Early Warning System

Riyanto, examiner

Abstrak

[ABSTRAK
Perancangan VLSI dengan hybrid VHDL merupakan metode desain untuk menghasilkan Sistem On Chip yang berbasis FPGA Xilinx Spartan 3. Sistem yang di desain adalah arsitektur CPU yang terdapat di Ocean Bottom Unit (OBU) Tsunami Early Warning System. Proses desain di implementasikan pada FPGA board Xilinx Spartan 3.
Perancangan VLSI CPU OBU dengan metode hybrid VHDL di lakukan dengan urutan proses desain yaitu membuat kode VHDL untuk menyimpan data pengukuran dan mengolah dengan algoritma mofjeld, Mengubah kode VHDL menjadi RTL, Mengubah RTL menjadi schematic dan kode verilog, Mengubah verilog menjadi CMOS layout, Menggunakan kode VHDL sebagai configure device pada XC3S200, genetrate PROM file pada XCF02S.
Hasil rancangan adalah VLSI 0,25 μm pada CPU OBU dengan jumlah gerbang logika yang digunakan sebanyak 699 buah dan 347 buah flipflop. Sedangkan dalam teknologi VLSI kapasitas adalah 10k -1M. Dengan metode hybrid VHDL jumlah gate pada desain CPU OBU masih dapat ditingkatkan dengan cara meningkatkan memori simpan sebanyak mungkin.;VLSI design with a hybrid VHDL is a design methods to produce a System
On Chip based on CMOS layout. The designed system is CPU architecture located on Ocean Bottom Unit Tsunami Early Warning System. The design process implemented on Xilinx Spartan 3 FPGA board.
Design of VLSI OBU CPU with a hybrid VHDL method is done by order of the design process is to make VHDL code for storing and processing the measurement data with the algorithm mofjeld, Changing the VHDL code into RTL, Changing RTL into schematic and verilog file, Changing verilog code into CMOS layout, Using the VHDL code as configure devices on the XC3S200, generating PROM files on XCF02S Xilinx Spartan.
The design results is VLSI 0,25 μm in CPU OBU with 699 logic gates and 347 flip-flops. While in VLSI technology the capacity is 10k-1M. With a hybrid method the gate of CPU OBU can be increased by increasing the memory as much as possible.;VLSI design with a hybrid VHDL is a design methods to produce a System
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