Disain dan implementasi field-programmable gate array untuk identifikasi citra wajah menggunakan artificial neural networks

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Abstrak

[ABSTRAK
FPGA merupakan piranti yang bersifat dapat dikonfigurasi-ulang (reconfigurable). Dengan mengambil keuntungan dari paralel hardware, eksekusi FPGA dapat lebih cepat dari pemrosesan DSP(Digital Signal Processor). Disain dan Implementasi Pengenalan wajah menggunakan FPGA, untuk mengidentifikasi citra wajah yang diberikan dengan menggunakan Fitur utama dari wajah. Dalam tesis ini Algoritma Artificial Neural Network metode Back Propagation disajikan, untuk mendeteksi pandangan frontal wajah. Extraksi Penciri citra wajah di lakukan dengan (PCA) dan identifikasi menggunakan Back Propagation. Citra wajah diambil dari 100 At&T Database menghasilkan 90 % acceptance ratio.
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<B>ABSTRACT
FPGA is a device that can be re-configured (reconfigurable). By taking advantage of parallel hardware, FPGA execution can be faster than processing DSP (Digital Signal Processor). Design and Implementation of face recognition using FPGA, to identify a given face image using the main features of the face. In this thesis Algorithm Artificial Neural Network Back Propagation method is presented, for detecting frontal view faces. Identifier face image extraction is done by (PCA) and identification using Back Propagation. 100 face images taken from At & T database generates 90% acceptance ratio.;FPGA is a device that can be re-configured (reconfigurable). By taking advantage of parallel hardware, FPGA execution can be faster than processing DSP (Digital Signal Processor). Design and Implementation of face recognition using FPGA, to identify a given face image using the main features of the face. In this thesis Algorithm Artificial Neural Network Back Propagation method is presented, for detecting frontal view faces. Identifier face image extraction is done by (PCA) and identification using Back Propagation. 100 face images taken from At & T database generates 90% acceptance ratio.;FPGA is a device that can be re-configured (reconfigurable). By taking advantage of parallel hardware, FPGA execution can be faster than processing DSP (Digital Signal Processor). Design and Implementation of face recognition using FPGA, to identify a given face image using the main features of the face. In this thesis Algorithm Artificial Neural Network Back Propagation method is presented, for detecting frontal view faces. Identifier face image extraction is done by (PCA) and identification using Back Propagation. 100 face images taken from At & T database generates 90% acceptance ratio., FPGA is a device that can be re-configured (reconfigurable). By taking advantage of parallel hardware, FPGA execution can be faster than processing DSP (Digital Signal Processor). Design and Implementation of face recognition using FPGA, to identify a given face image using the main features of the face. In this thesis Algorithm Artificial Neural Network Back Propagation method is presented, for detecting frontal view faces. Identifier face image extraction is done by (PCA) and identification using Back Propagation. 100 face images taken from At & T database generates 90% acceptance ratio.]