

Variation tolerant on-chip interconnects

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Abstrak

This book presents design techniques, analysis and implementation of high performance and power efficient, variation tolerant on-chip interconnects. Given the design paradigm shift to multi-core, interconnect-centric designs and the increase in sources of variability and their impact in sub-100nm technologies, this book will be an invaluable reference for anyone concerned with the design of next generation, high-performance electronics systems.