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# ISTFA 2003: Proceedings of the 29th International Symposium for Testing and Failure Analysis, 2-6 November 2003, Santa Clara, California

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#### **Abstrak**

#### Contents:

- Session 1: Advanced Techniques
- Scanning Magnetoresistive Microscopy for Die-Level Sub-Micron Current Density Mapping
- High Resolution Current Imaging by Direct Magnetic Field Sensing
- Fault Isolation of High Resistance Defects using Comparative Magnetic Field Imaging
- High Resolution Backside Thermography using a Numerical Aperture Increasing
  Lens
- Session 2: Optical Techniques
- Study of Critical Factors Determining Latchup Sensitivity of ICs using Emission Microscopy
- New Applications of Thermal Laser Signal Injection Microscopy (T-LSIM)
- PC Card Based Optical Probing of Advanced Graphics Processor using Time Resolved Emission
- Time-Resolved Optical Measurements from 0.13μm CMOS Technology Microprocessor using a Superconducting Single-Photon Detector
- IC Diagnostic with Time Resolved Photon Emission and CAD Auto-channeling
- Session 3: Package Level Analysis 1
- 3D X-ray Computed Tomography (CT) for Electronic Packages
- High-Angle Electron Microscopy Technique for Analysis of Thin Film Contamination on IC Package Exteriors
- Solder Bump Defects in Ceramic Flip Chip Packages and Their Acoustic Signatures.
- Copper Bond over Active Circuit (BOAC) and Copper over Anything (COA) Failure Analysis
- Investigation of Bond-pad Related Inter-metal Dielectric Crack
- Session 4: Sample Preparation 1
- Enhanced SEM Doping Contrast
- Interconnect and Gate Level Delayering Techniques for Cu/Low k Technology Failure Analysis
- Backside Deprocessing of CMOS SOI Devices for Physical Defect and Failure Analysis
- A Novel Approach to Front-side Deprocessing for Thinned Die after Backside

#### Failure Isolation

- Session 5: System Level Analysis
- Dynamic Infrared System Level Fault Isolation
- X-ray Laminography Benchmarking and Failure Analysis of Solder Joint Interfaces
- XRF Correlation of Board Reseats due to Intermittent Failures from the use of Thin Gold Plating finish on the Contact Fingers
- Session 6: Metrology and Materials Analysis 1
- Deal Time SEM Imaging of FIB Milling Processes for Extended Accuracy on TEM Samples for EFTEM Analysis
- A Method for Exact Determination of Dram Deep Trench Surface Area
- A Review of TEM Observations of Failures of the Memory Cell in a Deep Trench Capacitor DRAM
- The Effect of Tem Specimen Preparation Method on Ultra-thin Gate Dielectric Analysis
- Forward Scattered Scanning Electron Microscopy for Semiconductor Metrology and Failure Analysis
- Session 7: Failure Analysis Process
- Contributions of a Formal Analysis Metaprocess to Breakthrough Failure Analysis Results
- SRAM Failure Analysis Strategy
- VLSI Design for Functional Failure Analysis in the < 90 nm and Flip-chip era
- Identification of an IDDQ Failure Mechanism Using a Variety of Front and Backside Analytical Techniques
- Novel Application of Transmission Electron Microscopy and Scanning Capacitance Microscopy for Defect Root Cause Identification and Yield Enhancement
- Session 8: Metrology and Materials Analysis 2
- Contact Failure due to Particulate Defect in a 0.13 μm CMOS Process
- Microhardness Testing on Via Fill Material for Via In Pad Technology
- Application of ToF-SIMS to Airborne Organic Contamination Analysis
- Session 9: Test 1
- Yield-Modeling and Test Oriented Taxonomy of IC Structure Deformations
- Analysis of IC Manufacturing Process Deformations: An Automated Approach Using SRAM Bit Fail Maps
- Electrical Failure Analysis and Characterization of Leakage Paths Leading to Single Cell Failures in 128Mbit SDRAMs
- Session 10: Poster
- A Study on Fluorine-Induced Corrosion on Microchip Aluminum Bondpads
- Advanced Process Defect Detection by Using Dynamic Bias Condition and MCT Camera
- Via Chain Failure Analysis Using a Combination of E-Beam and Optical Beam

### **Techniques**

- ESD Failure Signature Differences in the Devices Core Logic and Protection Structures -- A Case Study
- ESD: Correlation between Electrical Signature and Failure Modes
- Semi-Automated Cross-Section Process for Complti-Face Perimeter Samples
- FIB Micro-pillar sampling of Si devices and its 3D observation
- Recent Developments in Automated Sample Preparation for FESEM
- Wet Delineation of SEM Samples having Cu Interconnects
- An Evolution in Plastic Decapsulation Process Improvement
- Near IR Continuous Wavelength Spectroscopy of Photon Emissions from Semiconductor Devices
- Defect Isolation and Characterization in Contacts by Using Primary Voltage Adjustment