

## Design and test for multiple Gbps communication devices and systems

Deskripsi Lengkap: <https://lib.ui.ac.id/detail?id=20452728&lokasi=lokal>

---

### Abstrak

#### Contents :

- Part I: Overview
- High-Speed I/O Design and Test Review: From the Perspectives of Moore's Law and Multiple Gbps Data Rates
- Part II: System Architecture and Performance
- Transfer Functions for the Reference Clock Jitter in a Serial Link: Theory and Applications
- Channel Compliance Testing Utilizing Novel Statistical Eye Methodology
- Advances in High-Speed Design in Dispersively Attenuating Environments Such as Cables and Backplanes
- Part III: Design Simulation and Modeling
- Static Crosstalk Analysis
- Modeling Loss and Jitter in High-Speed Serial Connects
- Design and Modeling Methodology for High-Performance Power Distribution Systems
- Source Synchronous Bus Design and Timing Analysis for High-Volume Manufacturable System Interconnects
- Part IV: Design for High Performance
- Eye Opening Techniques Enabled by Dispersion Compensation
- Maximizing 10-Gbps Transmission Path Length in Copper Backplanes with and without Transceiver Technology
- How to Make Optimal Use of Signal Conditioning in 40-Gbps Copper Interconnects
- Design of a 6.25-Gbps Backplane SerDes with Top-Down Design Methodology
- A Flexible Serial Link for 5-10 Gbps in Realistic Backplane Environments
- Part V: Characterization and Test
- Signal Integrity and Jitter: How to Measure Them Correctly
- A Statistical and System Transfer Function Based Method for Jitter and Noise in Communication Design and Test
- Total Jitter Measurement at Low Probability Levels, Using the Optimized BERT Scan Method
- Comparison and Correlation of Signal-Integrity Measurement Techniques
- Performance Evaluation of High-Speed Serial Links

- Physical-Layer Design and Characterization of a 3.2 Gbps/Pair Memory Channel
- Acronym Guide