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Multi-run Memory Tests for Pattern Sensitive Faults

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Abstrak

This book describes efficient techniques for production testing as well as for periodic maintenance testing (specifically in terms of multi-cell faults) in modern semiconductor memory. The author discusses background selection and address reordering algorithms in multi-run transparent march testing processes. Formal methods for multi-run test generation and many solutions to increase their efficiency are described in detail. All methods presented ideas are verified by both analytical investigations and numerical simulations.

Provides the first book related exclusively to the problem of multi-cell fault detection by multi-run tests in memory testing process;
Presents practical algorithms for design and implementation of efficient multi-run tests;
Demonstrates methods verified by analytical and experimental investigations.