Improved floating point multiplier design based on canonical sign digit

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Abstrak

Improved floating point (FP) multiplier based on canonical signed digit code (CSDC) has been reported in this paper. Array structure was implemented through Hatamain's scheme of partial product generation along with Baugh-Wooley's (B.W) sign digit multiplication technique. Moreover, CSDC approaches were used for the addition of partial products in constant time without carry propagation and independent of operands. The functionality of these circuits was checked and performance parameters, such as propagation delay, dynamic switching power consumptions were calculated by spice spectre using 90nm CMOS technology. Implementation methodology ensures the stage reduction for floating point multiplier, hence substantial reduction in propagation delay compared with B.W.'s methodology, has been investigated. Implementation result offered propagation delay of the single precision floating point multiplier was only ~14.7ns propagation delay while the power consumption of the same was ~23.7mW. Almost ~40% improvement in speed from earlier reported FP multiplier, e.g. B.W implementation methodology, the best architecture reported so far, has been achieved.