Vlsi circuit optimization for 8051 mcu

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Abstrak

With the aid of Electronic Design Automation tools, we perform circuit optimization on the 8051 microcontroller. The original 8051 microcontroller operates at a clock frequency 12 MHz, and it was designed based on 3.5-µm process technology. Hence, the device is slow and the chip size is large. To enhance the performance of the device and to minimize the die size, we used 90-nm technology in our design. We first performed optimization when mapping the RTL codes with the 90 nm standard cell libraries. Once the gate level netlist was generated, we developed the layout of the device by going through floor-planning, placement, and routing. We show that our new design is capable of operating at 150 MHz (i.e., 12.5 times faster than the original design), with a significant reduction in chip size (i.e., the total area is 77249.814850 µm2). The power consumption of the chip is 593.9899 µW, which is at least 32% lower than that of other 8051 derivatives.