The design of a high speed nonlinear feedback-based current comparator

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Abstrak

In this paper a new current comparator architecture is presented, which utilizes the concept of nonlinear feedback to speed up the operation. The analytical formulation for quantifying the effect of the feedback is put forward. The functionality of the proposed comparator is verified using simulations carried out on an Orcad Pspice tool using Taiwan Semiconductors Manufacturing Company (TSMC) 0.18 µm technology parameters. The resolution and delay are found to be ± 10 nA and 1.48 ns, respectively at a reference current of 1µA. The effects of parameter variations on the performance of the proposed comparator at different design corners is also studied. The usefulness of the proposed comparator is demonstrated through a 3-bit current mode flash Analog to Digital Converter (ADC) and its performance parameters are also calculated using simulations. The simulation results show that the 3-bit current mode flash Analog to Digital Converter exhibits no missing codes and has Differential Non-Linearity (DNL) of -0.25 Least Significant Bit (LSB) and Integral Non-Linearity (INL) of -0.19 LSB.