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A 2.3/3.3-GHz Dual Band Low Noise Amplifier for WiMAX Applications in Indonesia

TESIS

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0906644133

FAKULTAS TEKNIK
PROGRAM TEKNIK ELEKTRO
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Diajukan sebagai salah satu syarat untuk memperoleh gelar Magister Teknik

TAUFIQ ALIF KURNIAWAN
0906644133

FAKULTAS TEKNIK
PROGRAM STUDI TEKNIK ELEKTRO
KEKHUSUSAN DIVAIS ELEKTRONIKA
DEPOK
JULI 2011

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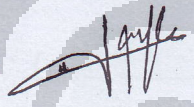
TandaTangan : 

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Telah berhasil dipertahankan di hadapan Dewan Penguji dan diterima sebagai bagian persyaratan yang diperlukan untuk memperoleh gelar Magister Teknik pada Program Studi Teknik Elektro, Fakultas Teknik, Universitas Indonesia.

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Tanggal : 4 Juli 2011

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KATA PENGANTAR

Puji syukur saya panjatkan kepada Tuhan Yang Maha Esa, karena atas berkat dan rahmat-Nya, saya dapat menyelesaikan tesis ini. Penulisan tesis ini dilakukan dalam rangka memenuhi salah satu syarat untuk mencapai gelar ganda (*Double Degree*) Magister Teknik Program Studi Teknik Elektro pada Fakultas Teknik Universitas Indonesia dan Master di *Department of Electrical Engineering* pada NTUST – National Taiwan University of Science and Technology, Taiwan.

Saya menyadari bahwa, tanpa bantuan dan bimbingan dari berbagai pihak, dari masa perkuliahan sampai pada penyusunan tesis ini, sangatlah sulit bagi saya untuk menyelesaikan tesis ini. Oleh karena itu, saya mengucapkan terima kasih kepada:

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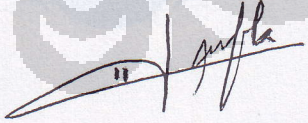

(Taufiq Alif Kurniawan)

ABSTRACT

To support the WiMAX infrastructure development in Indonesiaa dual-band 2.3/3.3 GHz low noise amplifier (LNA) is designed and analyzed. The LNA is designed by combining the inductive source degeneration architecture and the proposed switchable inductor for controlling gain. The chipis implemented by TSMC 0.18-µm CMOS technology.

First of all, the mathematical analysis of the proposed LNA architecture is conducted. It includesinput-impedance, gain and noise figure analysis. The proposed input-impedance analysis modifies the input impedance of the inductive source degeneration LNA architecture, includes devices selection to fulfill S_{11} requirement. Furthermore, the gain analysis is performed to explain the proposed switchable inductor structure for controlling gain. It shows that combining on-chip inductor paralleled with series bond-wire and on-board inductor will obtain a flatter gain for two bands of interest. The noise figure for source inductive degeneration LNA architecture is derived. The noise figure described by the derived equations agrees well with that obtained from the simulation.

Secondly, the proposed dual-band 2.3/3.3 GHz LNA is simulated. At low-band mode, simulated results show the maximum S_{21} of 18.69 dB, an S_{11} below -29 dB, and a flat noise figure of 2.3 ~ 2.33 dB from 2.3 to 2.4 GHz. The LNA presents the IIP_3 and the P1dB of -12.1 dBm and -23.3 dBm, respectively, while consuming 18.4 mW at 1.5 V power supply. At high-band mode, the simulation results show the S_{21} of 17.01 ~ 17.48 dB, the S_{11} below -21 dB, and an flat noise figure of 2.36 ~ 2.37 dB from 3.3 to 3.4 GHz. The LNA consumes only 12.9 mW at high-band mode, while exhibiting the IIP_3 and the P1dB of -11.3 dBm and -22.1 dBm, respectively.

And then, the proposed LNA is verified by the post-simulation in which the bond-wire effects are considered for an on-board deployment. At low-band mode, the post-simulation results show the S_{11} of -29.11 dB ~ -32 dB, the S_{21} of 17.18 ~ 17.42 dB, and the flat noise figure of 2.67 ~ 2.71 dB. The LNA exhibits the IIP_3 and P1dB of -13.4 dBm and -24.2 dBm respectively, while consuming 16.32 mW power. At high-band mode, the LNA exhibits the S_{21} of 15.5 ~ 15.88

dB, the S_{11} of -12.94 ~ -16.82 dB, and the flat noise figure of 2.52 ~ 2.54 dB while consuming 11.75 mW. The IIP_3 and P1dB for the high-band mode are -12.3 dBm and 23.3 dBm, respectively. The total chip area ofthe proposed LNA is 0.9 mm^2, including the IO pads.

Keywords: CMOS, Indonesia, inductive source degeneration, LNA, RF, switchable inductor, WiMAX.

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Taipei, Taiwan, June 2011

Taufiq Alif Kurniawan

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CHAPTER 1 INTRODUCTION

1.1 Worldwide Interoperability for Microwave Access (WiMAX)

Worldwide interoperability for microwave access (WiMAX) is a new wireless technology providing the broadband service and broad coverage of up to 70 km in line-of-sight (LOS) environments [1]. WiMAX is the commercialization of the IEEE 802.16 standard, an evolving standard initiated at the National Institute of Standards and Technology in 1998 [2]. Several active standards of WiMAX have been released by IEEE. The first released active standard of WiMAX was IEEE 802.16-2004 [3], addressed in the band between 2 - 11 GHz and 10 – 66 GHz for non-LOS and LOS environments, respectively. For the next standard, such as IEEE 802.16e, applications for mobility on notebooks and personal digital assistants were enabled within three narrow bands, namely 2.5-2.9 GHz, 3.4-3.6 GHz and 5.2-5.9 GHz.

WiMAX can serve as a backbone for the 802.11 hotspot and supports a wide variety of applications, as shown in Figure 1.1.1. In addition, the user can connect the mobile devices directly to the WiMAX base-station without using the wireless LAN. Users who connect their mobile devices directly to WiMAX base-station will approximately achieve a range up to 5 to 6 miles.

WiMAX is different from the IEEE standards 802.11a/b/g/n. The goals of WiMAX design are to provide a broadband internet access and to substitute the last mile wired-access networks for emerging market with no broadband access. Therefore, the user who did not have the LAN facility can now connect to internet via WiMAX easily. The other benefits of WiMAX application are the speed and low cost broadband access to markets in the rural areas or unwired countries. WiMAX can also be used in disaster recovery scenes where the wired networks have broken down [2]. WiMAX networks were installed to help recovery missions in several hurricane disasters.

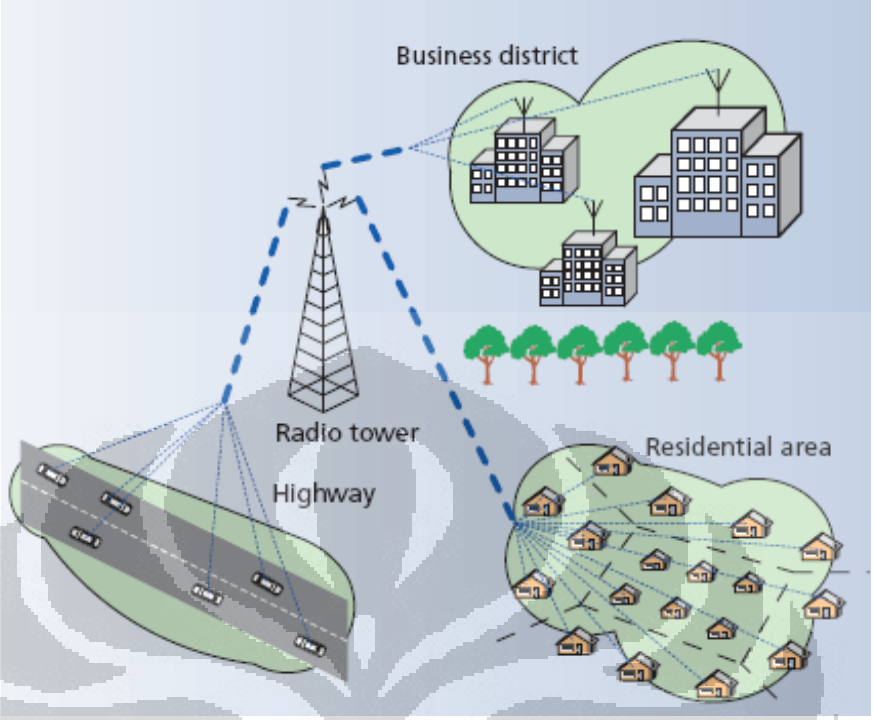


Fig. 1.1.1WiMAX applications [2]

1.2 WiMAX in Indonesia

In February 2010, WiMAX forum has announced that in the end of 2010, WiMAX service providers cover more than 823 million people[1]. In February 2011, WiMAX forum released that the network has been developed in 150 countries with 582 deployments, as shown in Fig. 1.2.1.

Red circles represent the areas where 802.16d is adopted for WiMAX, while blue ones representing those 802.16e are used. According to the frequency allocation shown in Fig. 1.2.1, the most popular deployments are in the frequency bands of 3.5 GHz (52.92%) and 2.5 GHz (19.24%).

[1]WiMAX forum Industry Research Report, March 2011

Fig.1.2.1WiMAX development in the world

As a big country with 250 million people, Indonesia is the potential market for WiMAX (4G). On January 19, 2008 the Indonesia government signed two ministry decrees and three regulations releasing spectrum at 2.3 GHz and 3.3 GHz for wireless broadband access across all regions of Indonesia. The decrees and regulations outline the migration of existing services at 3.4-3.6 GHz to 3.3 GHz in addition to new services at 2.3 GHz and 3.3 GHz. The 2.3 GHz frequency is divided to 15 zones of auction which are North, Central, and South Sumatra, Jabodetabek, West Java, Central, and East Java, Bali, Nusa Tenggara, Papua, Maluku and North Maluku, South and North Sulawesi, West and East Kalimantan, and the Riau Islands.

According to the statistics from Business Monitor International Report 2Q2008, the demand for 3G in Indonesia will increase significantly. As shown in Fig.1.2.2, in 2012 the number of consumers for 3G will be over 10 million and that for 4G will approach 10 million. In line with this, cellular telecommunication operators and CDMA operators in Indonesia showed deep interests to provide 4G services [4]. This situation encouraged Indonesia government to pay more attention to support local industries in WiMAX technology. The government unofficially announced that 2.3 GHz auction winner obligates to utilize at least 30% local content for substation and 40% for base-station as standard in WiMAX

Indonesia[2]. Some policies were issued, such as Ministerial Regulation No.Kominfo.7/PER/M.KOMINFO/01/2009 about Spatial Needs Radio Frequency Band for Wireless Broadband Services (Wireless Broadband).

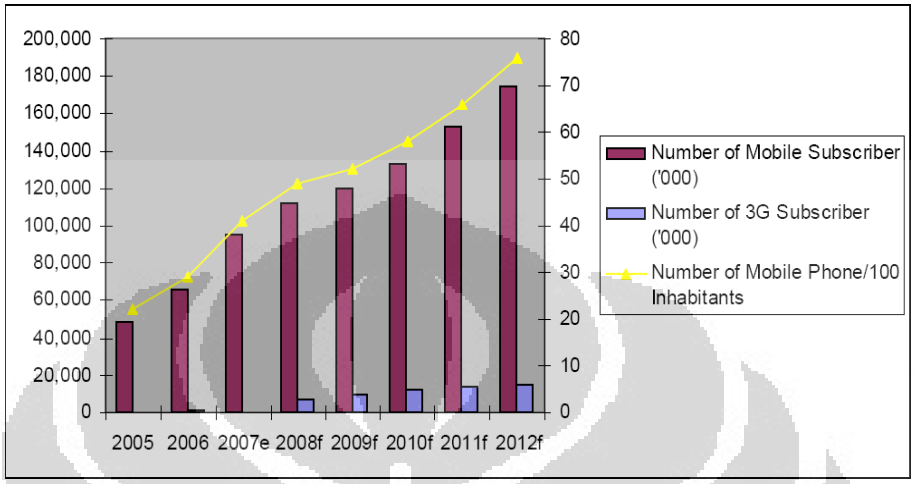


Fig.1.2.2 Indonesia telecommunication customer statistics

1.3 Research Motivation

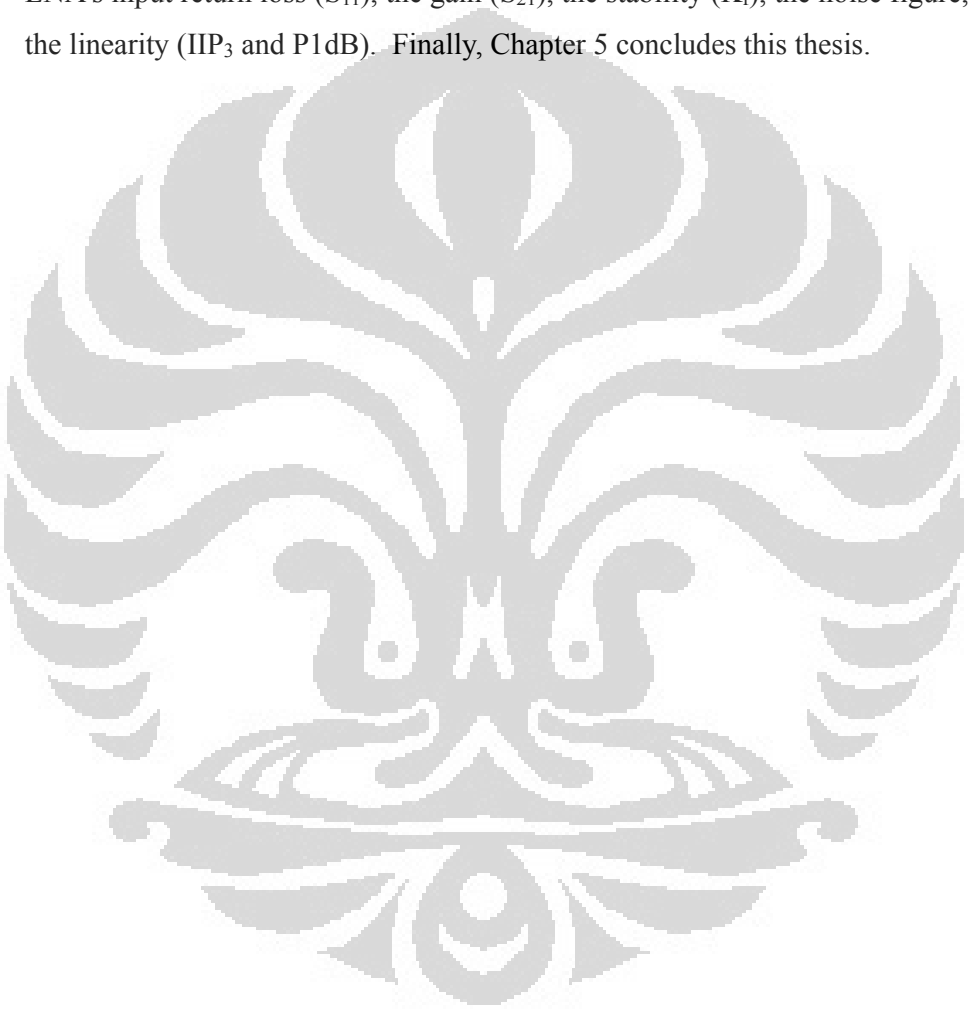
The motive of this research is to design a dual-band low noise amplifier (LNA) which operates at 2.3/3.3 GHz as one important component of the WiMAX receiver, especially for Indonesia. In this work, the narrow-band configuration is adopted because a wide-band LNA is vulnerable to interferences from undesired applications due to its limited linearity [5] and noise performance [6]. The conventional architecture uses two narrow band RF front-ends in parallel in the transceiver design [7]. Though this topology has good performance at either frequency band, it dissipates high power and requires a large chip size [8]. The other approaches adopting two difference input circuits [9] or a concurrent dual-band matching circuit [10] are more compact and consume smaller power than the conventional design. But they still occupy a large chip area because they employ many inductors. In this work, the dual-band LNA based on the conventional inductive source degeneration is designed using a switchable inductor in 0.18-µm technology.

[2]WiMAX Indonesia Conference 2009, Mr. Azhar Hasyim, Director of Telecom Standard, Ministry of information & Communication

1.4 Thesis Overview

This thesis is organized as follows. Chapter 2 provides the analysis of the LNA and the derived equations which are revised from the basic theory of the narrow-band LNA.

The next two chapters (Chapter 3 and Chapter 4) are devoted to the pre-layout simulation and the post-layout simulation results regarding the proposed LNA's input return loss (S_{11}), the gain (S_{21}), the stability (K_f), the noise figure, and the linearity (IIP_3 and P1dB). Finally, Chapter 5 concludes this thesis.



CHAPTER 2 BASIC THEORY of LOW NOISE AMPLIFIER

2.1 RF-Receiver Architecture

An RF receiver extracts the information from the received signal that is corrupted by noise in transmissions. It is desired that the output signal of the receiver is a replica of the modulated signal at the transmitter input [11]. As an example, the architecture of a receiver for the voice communications is shown in figure 2.1.1. The signal is amplified by a low-noise amplifier (LNA). Next the signal is down-converted to a lower frequency by a mixer to facilitate subsequent demodulation and then the demodulated output is amplified to drive the speaker.

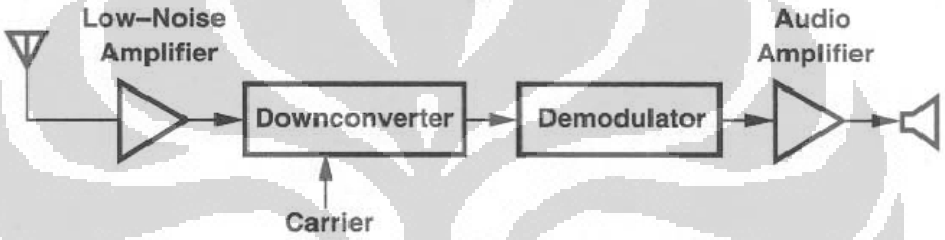


Fig. 2.1.1 Block diagram of a generic analog receiver RF system [12]

There are some fundamental parameters regarding an RF receiver, namely 1) carrier frequency, 2) channel bandwidth and spacing, 3) sensitivity, and 4) selectivity. Additionally, it is getting important to realize a receiver with low cost and low power consumption.

The first and second fundamental parameters of a receiver are regulated by IEEE standards, such as IEEE 802.16d for WiMAX and IEEE 802.11a for WLAN, Bluetooth for WPAN, or CDMA for 3G cellular phones. Allocation of frequency band, signal bandwidth, modulation scheme, data rate, channel assignment, and channel spacing are mandated by these standards [13].

Sensitivity specifies the minimum input signal power that the receiver can reliably detect the signal. The noise figure (NF) is defined as

$$NF = \frac{SNR_{in}}{SNR_{out}} \quad (2.1.1)$$

$$= \frac{P_{sig}/P_{RS}}{SNR_{out}} \quad (2.1.2)$$

$$P_{sig} = P_{RS}.NF.SNR_{out} \quad (2.1.3)$$

where P_{sig}denotes the input signal power density and P_{RS}denotes the source

resistance noise power density, both in mW per Hz. Then, for a flat channel,

$$P_{sig,tot} = P_{RS}.NF.SNR_{out}.B \quad (2.1.4)$$

where, B represents the signal bandwidth in Hz. Based on (2.1.3), it can be calculated in dBm as follows,

$$P_{in,min|dBm} = P_{RS|dBm/Hz} + NF|_{dB} + SNR_{min|dB} + 10.\log_{10} B \quad (2.1.5)$$

where $P_{in,min}$is the minimum input power that can lead to a minimum outputSNR_{min}. It can be seen that receiver sensitivity is related to the noise figure of the system.$P_{RS} = kT$, where k is the Boltzmann constant and T is temperature in Kelvin. At room temperature P_{RS} is approximately-174 dBm/Hz. Thus,

$$P_{in,min|dBm} = -174\frac{dBm}{Hz} + NF|_{dB} + SNR_{min|dB} + 10logB \quad (2.1.6)$$

The summation of the resistance noise power density (P_{RS}), Noise Figure *(NF)* and $10\,log_{10}\,B$ can be taken as the effective input noise power density (the noise floor, *F*).Hence,

$$P_{in,min|dBm} = SNR_{min|dB} + F \quad (2.1.7)$$

Selectivity in a receiver is defined as the maximum power level of interferer at which the receiver can still detect an input signal at 3 dB above the required sensitivity level. The selectivity parameter shows the capability of an RF receiver to process desired signal in strong interferers or channel blockers. Linearity of the receiver RF filter, the channel select filter and the local oscillator phase noise are used for measuring the receiver selectivity.

Power consumption and die cost have always been the design constraints that deserve serious considerations [12]. The last but not the least receiver parameters are image rejection and dynamic range. Image rejection is related to how good a receiver can suppress or cancel out the image signal appeared as blockers or interferers relative to the LO signal and degrade the SNR, while dynamic range is the ability of a receiver to accommodate a large input signal power range.

In RF design, the situation is more complicated. For simplicity, the bound of the dynamic range is determined by "spurious-free dynamic range" (SFDR) [14]. The upper bound of the dynamic range is defined as the maximum input level in a two-tone test in which the third-order intermodulation products do not

exceed the noise floor [14]. From IIP_3 calculation shown in Fig. 2.1.2,

$$P_{IIP_3} = P_{in} + \frac{P_{out} - P_{IM,out}}{2} \tag{2.1.8}$$

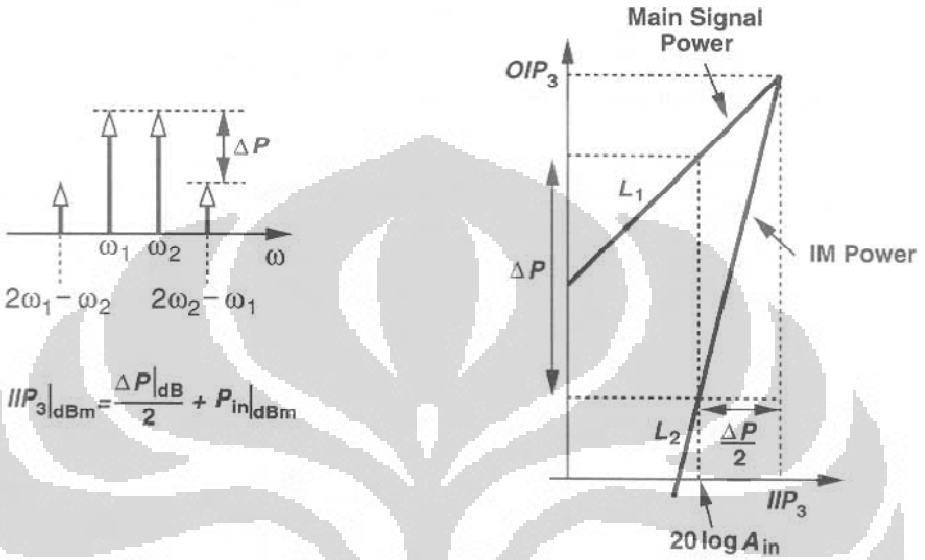


Fig. 2.1.2 Calculation of IP_3 without extrapolation and graphical interpretation

where $P_{IM,out}$ denotes the power of IM_3 components at the output. $P_{out} = P_{in} + G$ and $P_{IM,out} = P_{IM,in} + G$, where G is the circuit's power gain in dB and $P_{IM,in}$ is the input-referred level of the IM_3 products,

$$P_{IIP_3} = P_{in} + \frac{P_{in} - P_{IM,in}}{2} \tag{2.1.9}$$

$$= \frac{3P_{in} - P_{IM,in}}{2} \tag{2.1.10}$$

thus,

$$P_{in} = \frac{2P_{IIP_3} - P_{IM,in}}{3} \tag{2.1.11}$$

In case the input referred level of the *IM* product ($P_{IM,in}$) is equal to the noise floor (F), then

$$P_{in,max} = \frac{2P_{IIP_3} - F}{3} \tag{2.1.12}$$

The "spurious-free dynamic range" is the difference between $P_{in,max}$ and $P_{in,min}$:

$$SFDR = \frac{2P_{IIP_3} + F}{3} - (F + SNR_{min}) \tag{2.1.13}$$

$$= \frac{2P_{IIP_3} - F}{3} - SNR_{min} \qquad (2.1.14)$$

2.1.1 Heterodyne Receiver

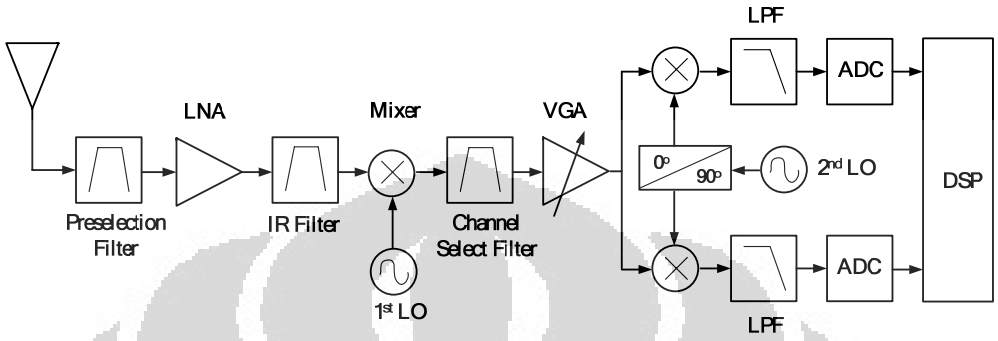


Fig. 2.1.3 Heterodyne receiver topology

Heterodyne receiver architecture is the most widely used architecture in wireless transceiver so far. In its operation, there are two down conversion, RF to IF and IF to baseband signal. From the incoming RF signal, the pre-selection filter removes out-of-band signal energy and partially reject the image signals. Next, the signal is amplified by the LNA to alleviate the contribution of noise from the succeeding stages. IR (Image Rejection) filter attenuates the signals at image band frequencies. The signal is then down-mixing by LO_1 to IF band. The channel selection filter is a band-pass filter that the signal in the band of interest can pass through. It is critical in determining the sensitivity and the selectivity of a receiver. The second mixer conducts the second down conversion of IF signal into in-phase (I) and quadrature (Q) components in case of phase and frequency modulation. The low-pass filter after the second mixer provides the necessary anti-aliasing function for ADC.

The above observation indicates the interdependence of noise figure, IIP_3 and gain of each stage in the receiving path. Every mixer in the heterodyne architecture produces spurious components that are functions of the RF or IF signals and the corresponding oscillators [12] they may degrade the signal quality. Hence, the frequency planning of the receiver plays an important role in the overall system performance. Despite the complexity and a large number of external components, the good selectivity and sensitivity of a heterodyne architecture have made it the most popular RF receiver for many decades.

2.1.2 Homodyne Receiver

Homodyne receiver converts the channel of interest from RF to baseband (zero IF frequency) directly. This architecture is also known as Direct IF or Zero-IF architecture. As shown in Fig. 2.1.4, the down-conversion must provide orthogonal outputs for frequency and phase modulated signals to correctly extract the information.

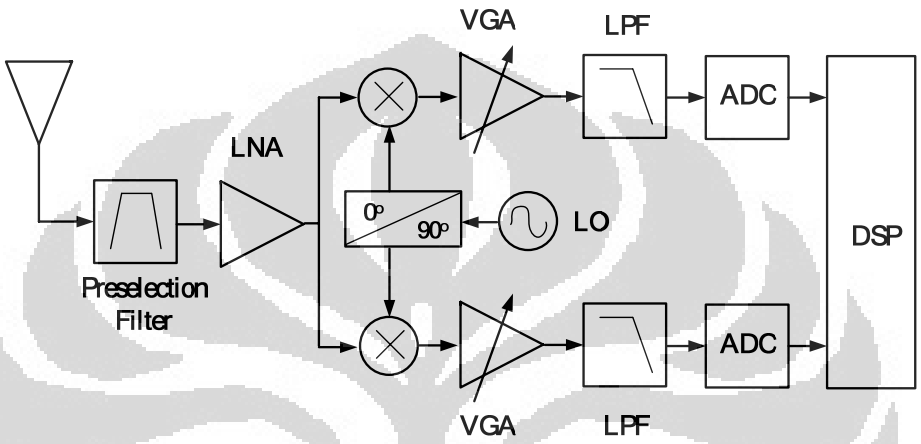


Fig. 2.1.4 Homodyne receiver topology

Although, the homodyne receiver architecture is simple, it offers two important advantages over a heterodyne architecture. First, the problem of image is circumvented since $\omega_{IF} = 0$, image filter is not required and the LNA need not possess output matching. Second, the low pass filter and the baseband amplifiers replace the IF channel select filter and the subsequent down-conversion stage in a heterodyne receiver.

Though homodyne receiver is simple, there are some practical reasons why homodyne receiver is not so popular as a heterodyne receiver. First, LO leakage due to imperfect isolation between mixer's LO port and the input port. This LO leakage will mix with the original LO to produce a DC offset in the mixer output and this offset may saturate the following stages in the receiver. Second, the error caused by DC offset can be a serious problem in the baseband section. Third, since the LO frequency and the received signal's frequency are the same, the LO power may leak the antenna. This may cause some EMI problems. Fourth, the flicker noise from active devices will contaminate the baseband signal.

2.2 Low Noise Amplifier

A low noise amplifier (LNA) is the first gain stage in the receiving path. In its design, there are several goals to be achieved, including minimizing noise figure, providing high gain with sufficient linearity, and providing matched input impedance, usually *50 Ω*, for terminating an unknown length of transmission line that delivers signal from antenna to amplifier [15]. The main function of an LNA is to provide sufficient gain to alleviate the noise contribution from the subsequent stages (such as mixer) [16]. However, the LNA itself should contribute as small amount of noise as possible. An LNA should accommodate a large dynamic-range input signal while produce insignificant distortion.

The minimum noise figure of a device can be obtained by finding the relations of the four noise parameters: G_c, B_c, R_n, G_u, and the optimum source admittance. Those parameters are derived from the classical two-port noise theory. However, in the LNA design, some trade-off should be considered. For example, the source impedance that maximizes the power gain differs from the source impedance that minimizes the noise figure. Therefore, it is possible for an LNA to possess bad input matching and poor gain, but a good noise figure.

Some analytic works are presented for the design strategy of an LNA to balance gain, input impedance, noise figure, and power consumption over the four noise parameters mentioned above. Consider the standard CMOS noise model shown in Fig. 2.2.1.

The dominant noise source in CMOS devices is channel thermal noise which can be modeled as a shunt current source in the output circuit of the device [16]. This excess noise may be attributed to the presence of hot electrons in the channel.

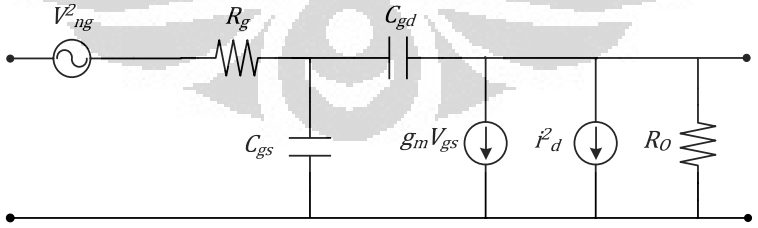


Fig. 2.2.1The standard CMOS noise model

The channel noise is given by,

$$\frac{\overline{i^2 d}}{\Delta f} = 4kT\gamma g_{d0} \qquad (2.2.1)$$

where$g_{d0}$is a zero-bias drain conductance of the device, and γ is a bias-dependent factor that, for long-channel devices, satisfies the inequality

$$\frac{2}{3} \leq \gamma \leq 1 \tag{2.2.2}$$

The value of one is valid when the drain-to-source voltage is zero, whereas the value of 2/3 is obtained when the device is in saturation region. However, for the short channel devices biased in saturation, gamma is much greater than 2/3 [17]-[20]. For 0.5-μm channel lengths, γ may be as high as 2/3, depending on bias condition [17].

The other noise source in MOS devices is the noise generated by the distributed gate resistance [21]. This noise source usually can be modeled as a series resistance in the gate circuit and an accompanying white noise generator [15]. For noise purposes, the distributed gate resistance is given by [15]

$$R_g = \frac{R_S W}{3n^2 L} \tag{2.2.3}$$

where R_S is the sheet resistance of the polysilicon, W is the gate width of the device, L is the gate length, and n is the number of gate fingers used to layout the device. The factor of 1/3 can be reduced to 1/12 by connecting gate fingers at both ends.

2.2.1 LNA Architecture

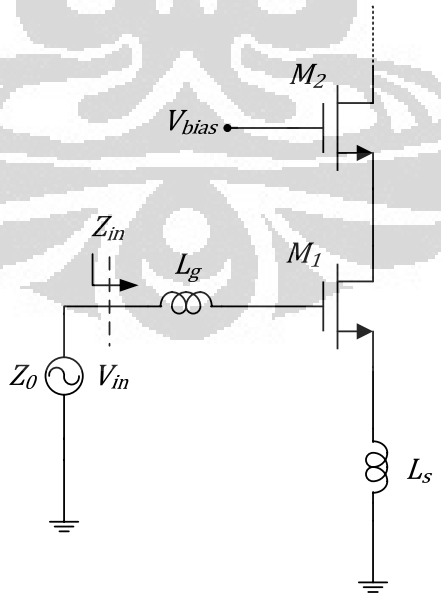


Fig. 2.2.2 Inductive source degeneration topology

Input matching is a technique to provide maximum power transfer to the system. There are some typical input matching circuits, such as resistive termination at the input port, common gate (CG) amplifier, resistive shunt-series feedback amplifier and inductive source degeneration topology [22]. Inductive source degeneration topology, shown in Fig. 2.2.2, is an LNA architecture that can have *50Ω* input impedance at the frequency of interest. It has the best noise performance in narrow-band LNA design [23] because this topology does not require additional noisy components.

At resonance frequency ω_0, the first-order analysis shows that the input impedance becomes

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs1}} + \left(\frac{g_{m1}}{C_{gs1}}\right)L_s \tag{2.2.4}$$

$$Imag(or\ Im)(Z_{in})\Big|_{\omega_0} = 0 \rightarrow Z_{in} = \left(\frac{g_{m1}}{C_{gs1}}\right)L_s \tag{2.2.5}$$

where ω_0 is resonance frequency, g_{m1} is transconductance of M1, C_{gs1} is M1's total gate-to-source capacitance.

The overall value of trans-conductance G_m of the input stage is proportional to the voltage on C_{gs1},

$$G_m = g_{m1}Q_{in} = \frac{g_{m1}}{\omega_0 C_{gs1}(R_s + \omega_T L_s)} \tag{2.2.6}$$

$$= \frac{\omega_T}{\omega_0 R_s(1 + \frac{\omega_T L_s}{R_s})} = \frac{\omega_T}{2\omega_0 R_s} \tag{2.2.7}$$

Q_{in} is the effective Q of the input circuit. The transconductance of this circuit at resonance frequency is independent of the device transconductance (g_{m1}) as long as the resonant frequency is maintained constant [15]. The transconductance of the stage will remain the same if the device width is along with the adjustment of L_g to maintain a desired frequency. Hence, when the gate width (and thus g_{m1}) is reduced, C_{gs1} is also reduced, resulting in an increased Q_{in} such that G_m remains unchanged.

Based on (2.2.6) and (2.2.7), a good design of LNA by selecting appropriate device width and bias point can lead to a good trade-off between the LNA parameters such as noise figure, gain, and power dissipation. Optimal size

of the input transistor can be determined as follows [15],

$$Q_L = \frac{\omega_0(L_s + L_g)}{R_s} = \frac{1}{\omega_0 R_s C_{gs}} \tag{2.2.8}$$

where Q_L is the effective Q of the device. We note that

$$C_{gs} = \frac{2}{3} W L C_{0x} \tag{2.2.9}$$

Hence,

$$W_{OPT} = \frac{3}{2\omega_0 L C_{ox} R_s Q_{L,OPT}} \tag{2.2.10}$$

The effective $Q_{L,OPT}$ of the input transistor for multi-standard LNA is around 4.5 (average of 3.5 and 5.5) in order to achieve very flat and low NF performance over the band of interest [24].

2.2.2 Switchable LNA for 2.3/3.3 GHz

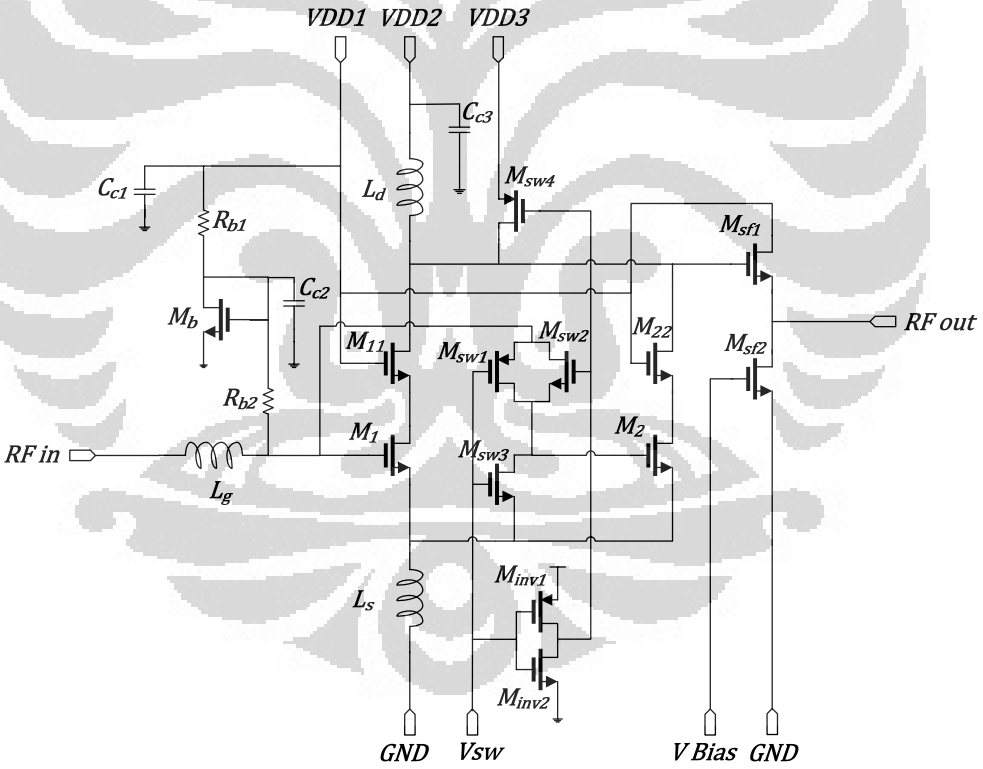


Fig.2.2.3 LNA for 2.3/3.3 GHz schematic

The proposed LNA schematic is illustrated in Fig. 2.2.3, where two parallel transistors are designed for dual band frequencies 2.3 and 3.3 GHz. Turning on the transmission gate equivalently increase the size of the common-source transistor (M1 and M2). This will move the resonance frequency from the

higher band (3.3 GHz) to the lower band (2.3 GHz).

The switchable inductor configuration as depicted in Fig. 2.2.4 is proposed to control the peak gain in this work. If M_{sw4} is switch-off, the peak gain determine by on-chip inductor (L_d) for low-band mode. Otherwise, the peak gain for high-band mode determines by bondwire in series with on-board inductor, as well as in parallel with L_d.

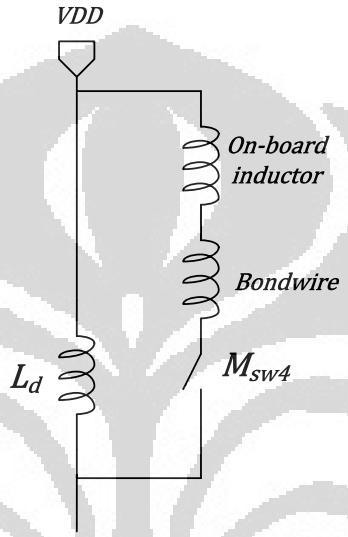


Fig. 2.2.4 Switchable inductor configuration

In this configuration, the on-resistance of M_{sw4} contributes parasitic resistance degrading the Q-factor of bondwire in series with on-board inductor. Hence, in switch-on case, the Q-factor of this series connection similar with the Q-factor of L_d enabling signals to pass through the parallel inductor connection. According to that reason, on-chip inductor in parallel with on-board inductor prefers to be implemented instead of another parallel combination (i.e. on-chip inductor in parallel with on-chip inductor or on-board inductor in parallel with on-board inductor) to obtain similar gain performance between both modes of the proposed LNA.

Size of the main transistors of the proposed circuit in Fig. 2.2.3 can be obtained by (2.2.12). For 3.3 GHz,

$$W_{OPT} = \frac{3}{2 * 2\pi 3.3e^{9} * 180e^{-9} * 8.45e^{-3} * 50 * 4.5} \qquad (2.2.11)$$

$$W_{OPT} \approx 204\ \mu m \qquad (2.2.12)$$

Similarly, for 2.3 GHz, $W_{OPT} \approx 290\ \mu m$.

According to (2.2.8), the gate-to-source capacitance can be calculated as follow,

$$C_{gs} = \frac{1}{\omega_0 R_s Q_L} \tag{2.2.13}$$

Hence with Q_L equal 4.5, C_{gs} for 3.3 and 2.3 GHz bands are 214.46 fF and 307.7 fF, respectively. Since 2.3-GHz configuration is obtained by parallely connecting two common source transistors (M1 and M2), the W_{OPT} for M2 in this topology can be calculated as,

$$C_{gs|2.3GHz} - C_{gs|3.3GHz} = \frac{2}{3} W_{OPT|M2} L C_{ox} \tag{2.2.14}$$

Therefore, the value of W_{OPT} for M2 is $91.9\mu m$, which is close to subtracting $204\ \mu m$ from $290\ \mu m$ in (2.2.12).

2.2.2.1 Input Impedance Analysis

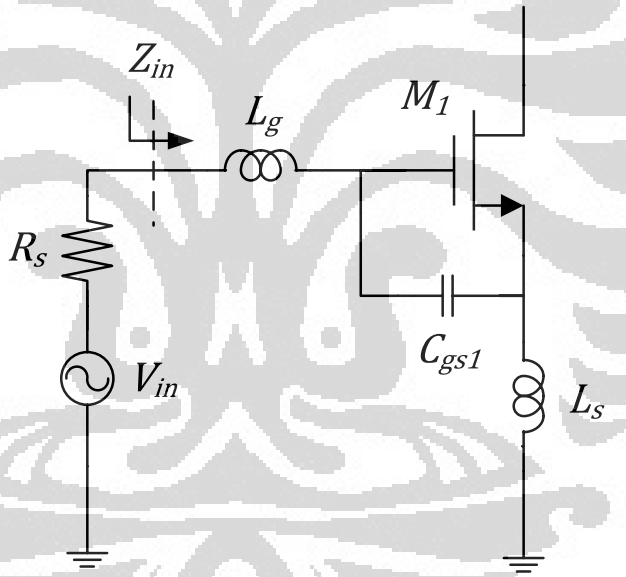


Fig. 2.2.5 Input impedance circuit

According to (2.2.4), the input return loss (S_{11}) of the proposed LNA can be expressed as follows,

$$S_{11} = \frac{Z_{in} - R_s}{Z_{in} + R_s} = \frac{s(L_g + L_s) + \frac{1}{sC_{gs1}}}{s(L_g + L_s) + 2.\frac{g_{m1} L_s}{C_{gs1}} + \frac{1}{sC_{gs1}}} \tag{2.2.15}$$

$$= \frac{s^2 + \frac{1}{C_{gs1}(L_g + L_S)}}{s^2 + 2.\frac{g_{m1}L_s}{C_{gs1}(L_g + L_S)}.s + \frac{1}{C_{gs1}(L_g + L_S)}} \quad (2.2.16)$$

g_{m1} is defined by,

$$g_{m1} = \frac{\partial I_D}{\partial V_{GS}}\Big|_{\mathrm{V_{DS,const}}} \quad (2.2.17)$$

where I_D is drain current, $V_{GS}$is gate-to-source voltage and V_{DS} is drain-to-source voltage.

Small signal model of the input stage along with a derivation of the input impedance for dual band 2.3/3.3 LNA is depicted in Fig. 2.2.6.

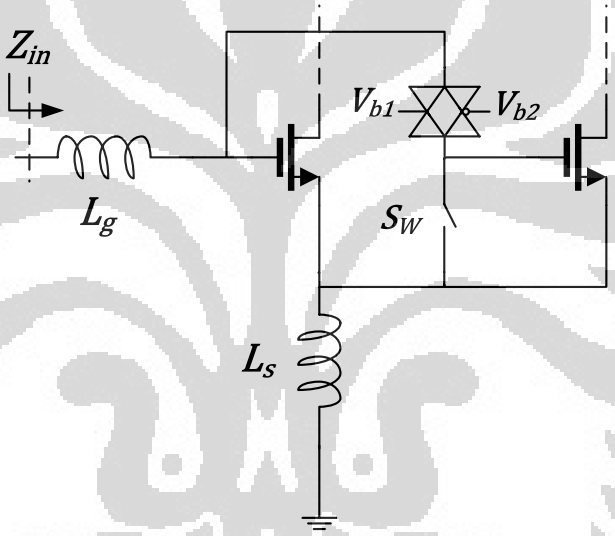


Fig. 2.2.6 Input matching for 2.3/3.3-GHz dual band LNA

When the transmission gate is on, the resonant frequency will be shifted to a lower band due to the increase of gate-to-source capacitance. For convenience, we assume that the on-resistance of the transmission gate can be neglected.

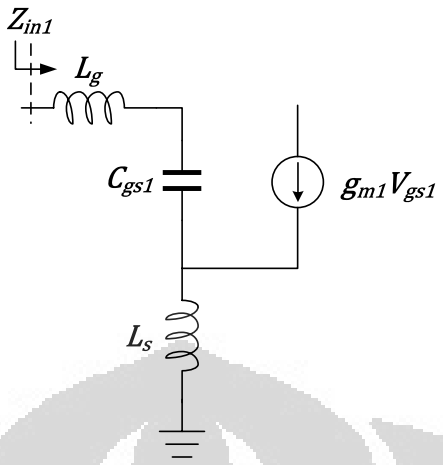


Fig. 2.2.7 Switch-off circuit model

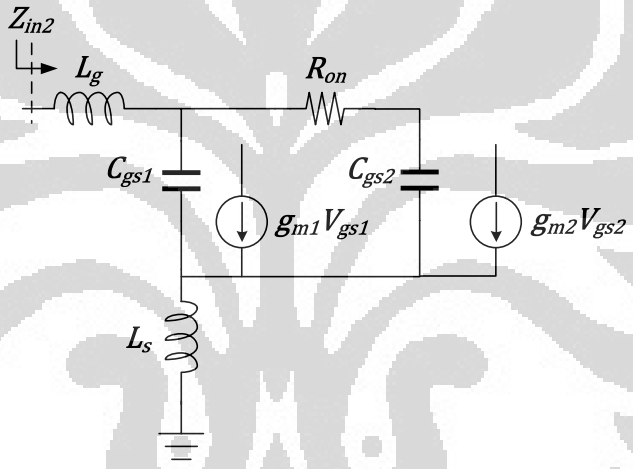


Fig. 2.2.8 Switch-on circuit model

As described previously, the input resistance of the source inductive degeneration topology is $(g_m/C_{gs})L_s = (g_{m1}/C_{gs1})L_s$ for the switch-off case shown in Fig. 2.2.7. For the switch-on case shown in Fig. 2.2.8, the input resistance becomes $[(g_{m1} + g_{m2})/(C_{gs1} + C_{gs2})]L_s$ = 50 ohm, where $g_m = (g_{m1} + g_{m2})$ is the equivalent transconductance and $C_{gs} = (C_{gs1} + C_{gs2})$ is the equivalent gate-to-source capacitance of two parallel-connected transistors.

In [5], the condition $\omega R_{on} C_{gs2} \ll 1$ is required such that the transmission gate's on-resistance has insignificant effect on the analysis. Hence, the following analysis holds for both 2.3 and 3.3 GHz bands.

2.2.2.2 Gain Analysis

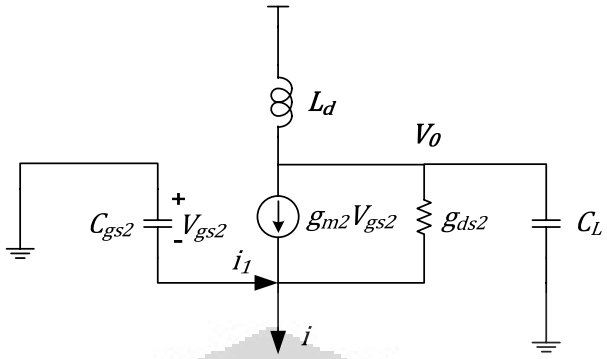


Fig. 2.2.9 Cascode transistor equivalent circuit model

We start the analysis of the cascode device first. The small signal model of the cascode device is shown in Fig. 2.2.9.

$$V_{gs2} = \frac{i_1}{C_{gs2}s} \tag{2.2.18}$$

$$g_{m2}V_{gs2} + i_1 + (V_0 + V_{gs2})g_{ds2} = i \tag{2.2.19}$$

Thus,

$$\left(\frac{g_{m2} + g_{ds2}}{C_{gs2}} + 1\right) i_1 + V_0 g_{ds2} = i \tag{2.2.20}$$

$$(i_1 - i)\frac{L_d s + r_{Ld}}{1 + (L_d s + r_{Ld})C_L s} = V_0 \tag{2.2.21}$$

where r_{Ld} is parasitic resistance of L_d. Next, (2.2.20) and (2.2.21) can be represented in matrix form,

$$\begin{bmatrix} g_{ds2} & \frac{g_{m2} + g_{ds2}}{C_{gs2}s} + 1 \\ -1 & \frac{L_d s + r_{Ld}}{1 + (L_d s + r_{Ld})C_L s} \end{bmatrix} \begin{bmatrix} V_0 \\ i_1 \end{bmatrix} = \begin{bmatrix} 1 \\ \frac{L_d s + r_{Ld}}{1 + (L_d s + r_{Ld})C_L s} \end{bmatrix} i \tag{2.2.22}$$

We then solve the transfer function of V_0 respect to i,

$$\frac{V_0}{i} = \frac{-(g_{m2} + g_{ds2})(L_d s + r_{Ld})}{(L_d s + r_{Ld})C_{gs2}g_{ds2}s + (g_{m2} + g_{ds2} + C_{gs2})(1 + (L_d s + r_{Ld})C_L s)} \tag{2.2.23}$$

where g_{m2} and g_{ds2} are transconductance and channel conductance of the cascode transistor. L_d, r_{Ld}, C_{gs2} and C_L are drain inductor, parasitic resistance on L_d, cascode transistor's gate-to-source capacitance and the parasitic capacitance at the output node of the LNA.

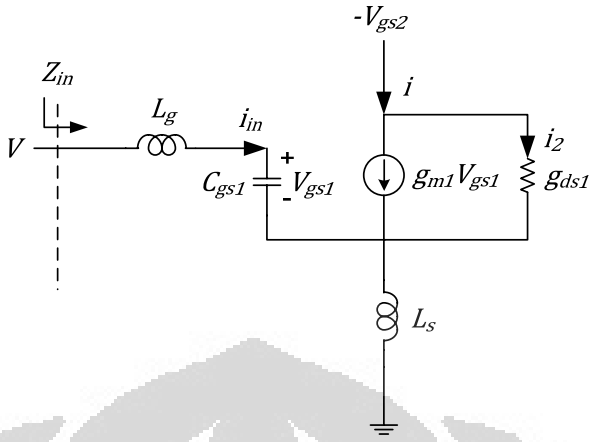


Fig. 2.2.10 Small signal of M1

After obtaining V_0/i value, the second step is to derive the transfer function of the common source transistor (M1) whose small-signal model is shown in Fig. 2.2.10. By KCL, i_2 can be expressed as,

$$i_2 = g_{ds1}\left(-V_{gs2} - \left(i + V_{gs1}C_{gs1}s\right)(L_S s + r_{Ls})\right) \tag{2.2.24}$$

where r_{Ls} is parasitic resistance of L_S. From (2.2.22),

$$i_1 = \frac{C_{gs2}s[(1 + (L_d s + r_{Ld})C_L s) + (L_d s + r_{Ld})g_{ds2}s]i}{(L_d s + r_{Ld})C_{gs2}s + (1 + (L_d s + r_{Ld})C_L s)\left(g_{m2} + g_{ds2} + C_{gs2}s\right)} \tag{2.2.25}$$

combining (2.2.18) and (2.2.25), we can obtain

$$V_{gs2} = \frac{\left[1 + (L_d s + r_{Ld})C_L s + (L_d + r_{Ld})g_{ds2}\right]i}{(L_d s + r_{Ld})C_{gs2}g_{ds}s + \left(1 + (L_d s + r_{Ld})C_L s\right)\left(g_{m2} + g_{ds2} + C_{gs2}s\right)} \tag{2.2.26}$$

Let,

$$A(s) = (L_d s + r_{Ld})g_{ds2}C_{gs2}s + \left(1 + (L_d s + r_{Ld})C_L s\right)\left(g_{m2} + g_{ds2} + C_{gs2}s\right) \tag{2.2.27}$$

$$D(s) = 1 + (L_d s + r_{Ld})C_L s + (L_d s + r_{Ld})g_{ds2} \tag{2.2.28}$$

Therefore, i_2 can be written as,

$$i_2 = -g_{ds1}\left(i\frac{D(s)}{A(s)}\right) + (i + i_{in})(L_S s + r_{Ls}) \tag{2.2.29}$$

hence,

$$i_2 = -g_{ds1}\left(i\left(\frac{D(s)}{A(s)} + (L_S s + r_{Ls})\right) + i_{in}(L_S s + r_{Ls})\right) \tag{2.2.30}$$

Refer to Fig. 2.2.10, by using KCL, we can derive

$$i_2 = i - i_{in}\frac{g_{m1}}{C_{gs1}s} \tag{2.2.31}$$

Therefore

$$i = \frac{i_{in}\left(g_{m1} - g_{ds1}C_{gs1}(L_S s + r_{Ls})s\right)}{\left[1 + g_{ds}\left(\frac{D}{A} + (L_S s + r_{Ls})\right)\right]C_{gs1}s} \tag{2.2.32}$$

The value of i_{in} can be derived by KVL in Fig. 2.2.10,

$$i_{in}\left((L_g s + r_{Lg}) + \frac{1}{C_{gs1}s}\right) + (L_S s + r_{Ls})(i_{in} + i) = V \tag{2.2.33}$$

where r_{Lg} is parasitic resistance of L_g.

Finally, input impedance of the circuit (Z_{in}) can be found as follows

$$Z_{in} = \frac{V}{i_{in}} = \{(L_g s + r_{Lg}) + (L_S s + r_{Ls})\} + \frac{1}{C_{gs1}s} + \frac{(L_S s + r_{Ls})\left(g_{m1} - g_{ds1}(L_S s + r_{Ls})C_{gs1}s\right)}{sC_{gs1}\left(1 + g_{ds1}\left(\frac{D}{A} + (L_S s + r_{Ls})\right)\right)} \tag{2.2.34}$$

Next, we ignore r_{Ld}, r_{Lg} and r_{Ls} because their values are very small.

Let ω_0 be the frequency of the gain peak where $1 - L_d C_L {\omega_0}^2 = 0$ and for input matching $1 - \{(L_g) + (L_S)\}C_{gs1}{\omega_0}^2 = 0$, thus

$$\frac{D(j\omega_0)}{A(j\omega_0)} = \frac{1}{j\omega_0 C_{gs2}} \tag{2.2.35}$$

By neglecting r_{Ld}, r_{Lg}, and r_{Ls}, (2.2.34) can be simplified as

$$Z_{in}(j\omega_0) = \frac{(j\omega_0 L_S)\{g_{m1} - g_{ds1}(j\omega_0 L_S)C_{gs1}.j\omega_0\}}{j\omega_0 C_{gs1}\left[1 + g_{ds1}\left(\frac{1}{j\omega_0 C_{gs2}} + j\omega_0 L_S\right)\right]} \tag{2.2.36}$$

Next, in order to obtain the real input impedance, *50Ω*, ${C_{gs1}\omega_0}^2$ is replaced by $1/(L_s + L_g)$ according to (2.2.4). Therefore, Z_{in} at the operating frequency can be determined as follows,

$$Z_{in}(j\omega_0) = \frac{L_S\left(g_{m1} + g_{ds1}\left(\frac{L_s}{L_s + L_g}\right)\right)}{C_{gs1}\left[1 - jg_{ds1}\left(\frac{1 - \frac{L_s C_{gs2}}{(L_g + L_s)C_{gs1}}}{\omega_0 C_{gs2}}\right)\right]} \tag{2.2.37}$$

By assuming that $g_{m1} \gg g_{ds1}$, $g_{ds1} \ll 1$, and $C_{gs2} \ll C_{gs1}$, the real input impedance (Z_{in}) in (2.2.37) similar with the simple expression in (2.2.5). Hence, the S_{11} can be expressed by (2.2.16).

From Fig. 2.2.10, let $Z_{in}(j\omega_0)$ be Z_0 from (2.2.36), i_{in} can be expressed as

$$i_{in} = \frac{V_{in}}{Z_0 + (L_g + L_S)s + \frac{1}{C_{gs1}s} + \frac{L_s(g_{m1} - g_{ds1}L_s C_{gs1}s^2)}{C_{gs1}\left(1 + g_{ds1}\left\{\frac{D}{A} + L_s s\right\}\right)}} \tag{2.2.39}$$

Combining (2.2.32) and (2.2.39), hence i can be expressed as,

$$i = \frac{V_{in}\left(g_{m1} - g_{ds1}L_sC_{gs1}s^2\right)}{\left(\left[1 + g_{ds1}\left(\frac{D}{A} + L_Ss\right)\right]C_{gs1}s\right)\left(Z_0 + (L_g + L_S)s + \frac{1}{C_{gs1}} + \frac{L_S\left(g_{m1} - g_{ds1}L_SC_{gs1}s^2\right)}{C_{gs1}\left(1 + g_{ds1}\left(\frac{D}{A} + (L_S)s\right)\right)}\right)} \quad (2.2.40)$$

Recall that $C_{gs1}{\omega_0}^2 = 1/(L_S + L_g)$,

$$i = \frac{V_{in}\left(g_{m1} - g_{ds1}L_SC_{gs1}s^2\right)}{\left(\left[1 + g_{ds1}\left(\frac{D}{A} + L_Ss\right)\right]C_{gs1}s\right)\left(Z_0C_{gs1}s + \frac{s^2}{{\omega_0}^2} + 1 + \frac{L_Ss\left(g_{m1} - g_{ds1}L_SC_{gs1}s^2\right)}{\left(1 + g_{ds1}\left(\frac{D}{A} + L_Ss\right)\right)}\right)} \quad (2.2.41)$$

The overall transconductance becomes

$$\frac{i}{V_{in}} = \frac{g_{m1} - g_{ds1}C_{gs1}L_Ss^2}{\left[1 + g_{ds1}\left(\frac{D}{A}L_Ss\right)\right]\left[\frac{s^2}{{\omega_0}^2} + Z_0C_{gs1}s + 1\right] + L_Ss\left[g_{m1} - g_{ds1}C_{gs1}L_Ss^2\right]} \quad (2.2.42)$$

Continuing the analysis, the gain of the LNA can be obtained by combining (2.2.23) and (2.2.42).

$$\frac{V_0}{V_{in}} = \frac{-L_Ds(g_{m2} + g_{ds2})\left(g_{m1} - g_{ds1}L_SC_{gs1}s^2\right)}{[A + g_{ds1}(D + A(L_Ss)]} \cdot \frac{1}{\left[\frac{s^2}{{\omega_0}^2} + Z_0C_{gs1}s + 1\right] + A(L_Ss)\left(g_{m1} - g_{ds1}L_SC_{gs1}s^2\right)} \quad (2.2.43)$$

Then, by replacing $(s^2/{\omega_0}^2) + Z_0C_{gs1} + 1 = B(s)$

$$\frac{V_0}{V_{in}} = \frac{-L_ds(g_{m2} + g_{ds2})\left(g_{m1} - g_{ds1}L_SC_{gs1}s^2\right)}{A(B + L_Ssg_{m1}) + g_{ds1}\left[BD + AL_Ss\left(B - C_{gs1}L_Ss^2\right)\right]} \quad (2.2.44)$$

At the operating frequency (ω_0), A, B, and D are

$$A = -L_dC_{gs2}g_{ds2}{\omega_0}^2 \quad (2.2.45)$$

$$D = j\omega_0L_dg_{ds2} \quad (2.2.46)$$

$$B = j\omega_0Z_0C_{gs1} \quad (2.2.47)$$

Therefore (2.2.44) can be written as

$$\frac{V_0}{V_{in}} = \frac{-jL_d\omega_0(g_{m2} + g_{ds2})\left(g_{m1} + g_{ds1}\frac{L_s}{(L_s + L_g)}\right)}{\frac{-jL_d\omega_0C_{gs2}g_{ds2}}{(L_g + L_s)C_{gs1}}\left(Z_0C_{gs1}\right) + \frac{g_{ds1}L_dg_{ds2}Z_0}{(L_g + L_s)}\left(C_{gs2}L_S{\omega_0}^2 - 1\right)} \quad (2.2.48)$$

Finally, the voltage gain (A_v) of the LNA can be simplified as

$$\frac{V_0}{V_{in}} = \frac{-j(g_{m2} + g_{ds2})\left(g_{m1} + g_{ds1}\frac{L_s}{(L_s + L_g)}\right)}{(g_{ds1}C_{gs2}L_S{\omega_0}^2 - 2jC_{gs2}\omega_0 - g_{ds1})\frac{g_{ds2}Z_o}{(L_g + L_s)}} \qquad (2.2.49a)$$

in which, by assuming that $g_{m1} \gg g_{ds1}$and $g_{m2} \gg g_{ds2}$, the magnitude of voltage gain (A_v) can be further approximated by

$$\frac{V_0}{V_{in}} = \frac{-j(g_{m1}g_{m2})}{(g_{ds1}C_{gs2}L_s{\omega_0}^2 - 2jC_{gs2}\omega_0 - g_{ds1})\frac{g_{ds2}Z_0}{(L_g + L_s)}} \qquad (2.2.49b)$$

This indicates that A_v is mainly contributed by transconductance of M1 and M2. Note that ${\omega_0}^2 = 1/(L_dC_L)$, hence the center frequency (ω_o) of the peak gain is determined by L_d and C_L.

2.2.2.3 Noise Figure Analysis

The other important parameter of LNA is the noise figure (NF) [15]. As depicted in Fig. 2.2.11, the equivalent noise model from source inductive degeneration LNA topology can be written as

$$Z_{in} = r_{Lg} + r_g + r_{nqs} + r_{ss} + r_{Ls} + \frac{g_{m1}L_S}{C_{gs}} \qquad (2.2.50)$$

where r_{Lg}, r_g, r_{nqs}, r_{ss}, r_{Ls} are gate inductor (L_g) resistance, gate resistance, non-quasi static effect of the transistor, source resistance, and source inductor (L_S) resistance, respectively. The non-quasi effect occurs when high frequency is applied to the gate [25]. Complete noise model equivalent circuit for the inductive source degeneration configuration shown in Fig. 2.2.11.

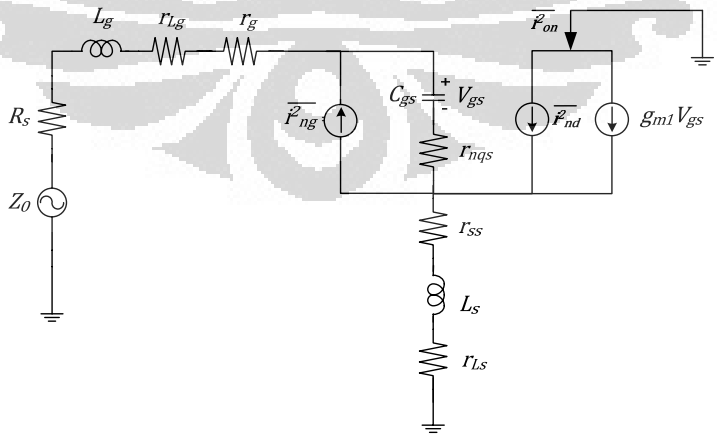


Fig. 2.2.11 Noise model of inductive source degeneration configuration

According to [25] there is a lot of controversy on the excess thermal noise

in short channel MOSFETs and the large enhancement is not observed in the devices of 0.18-um technology. The excess factor for 0.18-μm n-channel MOSFET does not exceed two at strong inversion and the excess factor is converged into several groups [26]-[29].

The basic frame of high frequency noise modeling of the field-effect transistor (FET) was first described by Van der Ziel in [30]. Van der Ziel showed the intrinsic noise effect could be represented by two noise generators, the drain noise current and the induced gate one. These noise currents are partially correlated with each other because they are generated from the same physical origin, i.e., thermal fluctuation of carriers in the channel. However, Van der Ziel's model cannot be applied to short-channel MOSFETs since the model does not account for the velocity saturation effect.

Some previous works [16, 31, 32] modeled the noise sources for RF CMOS transistors as:

$$\overline{\imath^2_{nd}} = 4kT\gamma g_{d0} \tag{2.2.51}$$

$$\overline{\imath^2_{ng}} = \frac{4kT\delta\omega^2 {C_{gs}}^2}{5g_{d0}} \tag{2.2.52}$$

where, $g_{d0} = (g_m/\alpha)$ represents the MOSFET output conductance at zero drain-source bias, for short channel $\alpha \leq 1$ [15]. γ, δ are the coefficients of transistor's channel noise and gate noise, respectively. For simplicity, the shunt noise current in (2.2.53) can be written by,

$$\overline{\imath^2_{ng}} = 4kT\delta g_g \tag{2.2.53}$$

where $g_g = \omega^2 {C_{gs}}^2/5g_{d0}$ (shunt conductance). However, in the gate noise expression, g_g is proportional to ω^2; hence the gate noise is not white [15]. Because of its monotonically increasing power spectral density, it is better to describe the gate noise as a blue noise. Furthermore, noisy gate current may negligible at low frequencies [16, 30], hence the noisy gate current will be ignored in this work.

Recall that the noise factor for an amplifier is defined as

$$F = \frac{(S/N)in}{(S/N)out} = \frac{Total\ output\ noise\ power}{Total\ output\ noise\ due\ to\ the\ input\ source\ resistance} \tag{2.2.54}$$

First, the transconductance of the circuit of the input stage is evaluated to make sure that the output noise of the LNA is driven by a *50-Ω* source.

$$G_m = g_{m1}Q_{in} = \frac{g_{m1}}{C_{gs1}(L_g + L_S)s^2 + (C_{gs}R_S + L_S g_{m1})s + 1} \quad (2.2.55)$$

$$= \frac{g_{m1}}{\frac{S^2}{{\omega_0}^2} + C_{gs1}(R_S + \omega_T L_S)s + 1} \quad (2.2.56)$$

$$= \frac{\omega_T}{\frac{1}{C_{gs1}}\left(\frac{S^2}{{\omega_0}^2} + 1\right) + (R_S + \omega_T L_S)s} \quad (2.2.57)$$

$$G_m(j\omega_0) = \frac{\omega_T}{j\omega_0(R_S + \omega_T L_S)} \quad (2.2.58)$$

$$= \frac{\omega_T}{j\omega_0 R_S(1 + \frac{\omega_T L_S}{R_S})} = \frac{\omega_T}{2j\omega_0 R_S} \quad (2.2.59)$$

where Q_{in} is effective Q of the amplifier's input circuit. In this equation, r_{Lg} and $r_g$are neglected because they are much less than the source resistance, R_S. As long as the resonant frequency is maintained constant, the transconductance of the circuit at resonance is independent of g_{m1}as shown in 2.2.59.

Consider the power spectral density of the dominant noise contributor of LNA, the channel current noise given in (2.2.51). It can be derived that the output noise power spectral density arising from this source is

$$S_{o,i_{nd}}(\omega_0) = 4kT\gamma g_{d0} \quad (2.2.60)$$

In addition, the output noise power spectral density due to the input source resistance($S_{o,SR}(\omega_0)$)can be written by,

$$S_{o,SR}(\omega_0) = S_{SR}(\omega_0){G_{m,eff}}^2 = \frac{4kT{\omega_T}^2}{{\omega_0}^2 R_S\left(1 + \frac{\omega_T L_S}{R_S}\right)^2} \quad (2.2.61)$$

Then, the output noise power spectral density due to parasitic resistance($S_{o,r_{par}}(\omega_0)$)can be represented by

$$S_{o,r_{par}}(\omega_0) = S_{r_{par}}(\omega_0){G_{m,eff}}^2 \quad (2.2.62)$$

$$= \frac{4kT(r_{Lg} + r_g + r_{SS} + r_{Ls}){\omega_T}^2}{{\omega_0}^2{R_S}^2\left(1 + \frac{\omega_T L_S}{R_S}\right)^2} \quad (2.2.63)$$

where parasitic resistance (r_{par}) are summation of the r_{Lg}, r_g, r_{SS} and r_{Ls}.

If the gate noise is neglected, the total output noise power density is the sum of (2.2.60), (2.2.61) and (2.2.63). Therefore, the noise factor of the proposed

LNA can be approximated by:

$$F = 1 + \frac{r_{Lg} + r_g + r_{SS} + r_{Ls}}{R_S} + 4\gamma g_{d0} R_S \left(\frac{\omega_0}{\omega_T}\right)^2 \qquad (2.2.64)$$

This equation for noise factor reveals several important features of this proposed LNA architecture. Note that the dominant term in (2.2.64) is the last term, which arises from channel thermal noise. Surprisingly, this term is proportional to g_{d0}. Hence, according to this expression, by reducing g_{d0} without modifying ω_T, we can simultaneously improve noise figure and reduce power dissipation. We achieve this result by scaling the width of the device while maintaining constant bias voltages on its terminals and leaving the channel length unchanged. Furthermore, reduction in g_{d0} (and, hence in C_{gs}) must be compensated by an increase in L_g to maintain a constant resonant frequency. Therefore, better noise figure performance and reduced power dissipation can be obtained by increasing the Q of the input circuit resonance (Q_{in}).

CHAPTER 3 – PRE-LAYOUT SIMULATION

3.1 The proposed 2.3/3.3 GHz Low Noise Amplifier Circuit

3.1.1 Test-bench Circuit

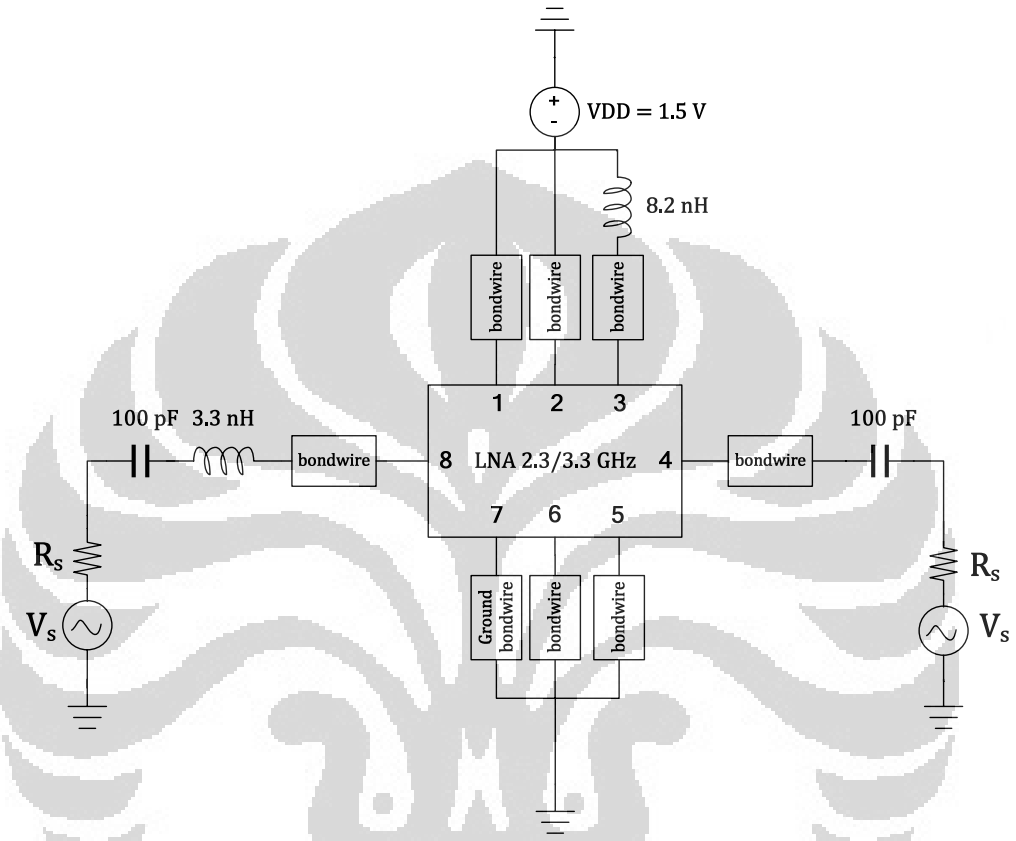


Fig. 3.1.1 Test-bench circuit

The schematic test-bench of the proposed LNA is shown in Fig. 3.1.1. It consists of 8 pins, namely VDD1, VDD2, VDD3, RF_OUT, VBIAS, VSW, GND, and RF_IN, respectively. In order to connect the proposed LNA chip with pad, bondwire and ground bondwire are placed on test-bench circuit. A 3.3 nH inductor in this test-bench circuit is a element of input matching.

Fig. 3.1.2 and Fig. 3.1.3 are the equivalent circuits for considering parasitic effect of bondwire and ground bondwire, respectively. Its equivalent circuits are modeled by assuming that the Q-factor of a bondwire inductor is 60. Hence, the series parasitic resistance can be calculated by,

$$Q = \frac{\omega L}{r_s} \tag{3.1.1}$$

where Q, ω, L, r_s are quality factor of inductor, frequency of interest, the value of bondwire inductor, and the parasitic resistance of bondwire inductor. Based on the calculation in 3.1.1, the parasitic resistance of bondwire for 2.3 and 3.3 GHz can be determined simultaneously.

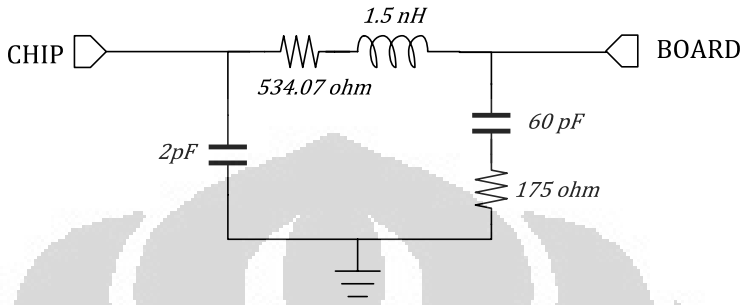


Fig. 3.1.2 Equivalent circuit for bondwire

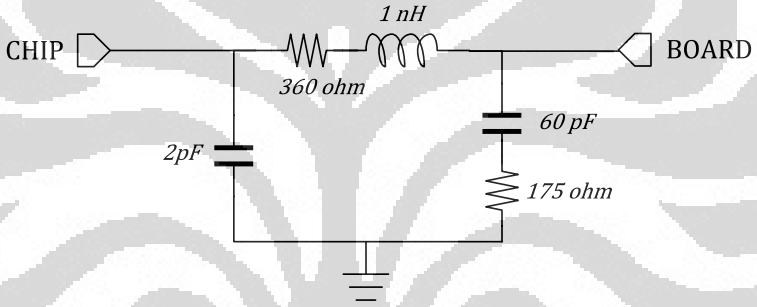


Fig. 3.1.3 Equivalent circuit for ground bondwire

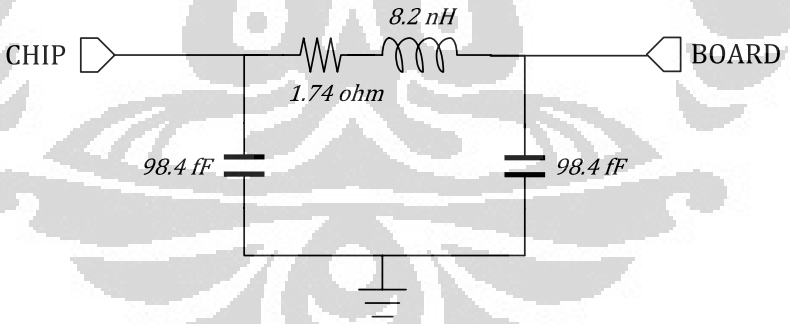


Fig. 3.1.4 Equivalent circuit for 8.2 nH on-board inductor

To demonstrate the parasitic effects of 8.2 nH on-board inductor, the equivalent circuit is shown in the Fig. 3.1.4. The parasitic resistance of the inductor is calculated by 3.1.1 with considering that Q-factor in 2.4 GHz is 71. Additionally, the parasitic capacitance of the inductor is determined by considering that its typical SFR (Self Resonance Frequency) is 5.6 GHz.

3.1.2 On-Chip 2.3/3.3 GHz LNA Circuit

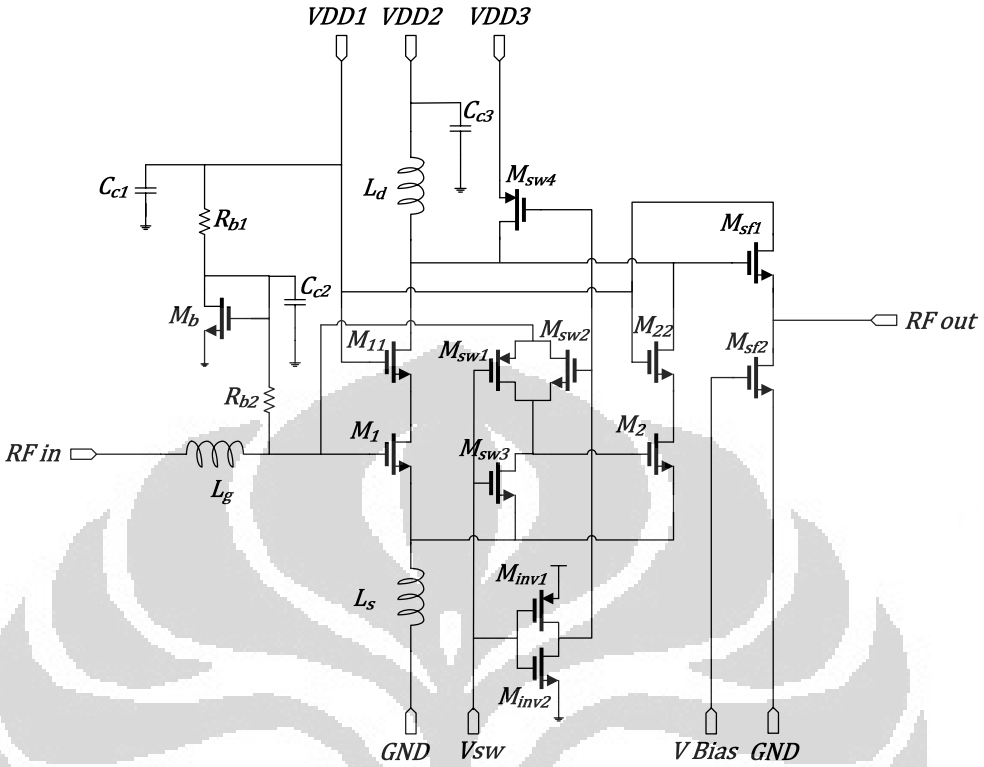


Fig. 3.1.5 A 2.3/3.3 GHz LNA schematic circuit

As depicted in Fig 3.1.5, two main transistorsM_1 and M_2 are separated with each other by a transmission gate (M_{sw1}, and M_{sw2}). The transmission gate controls mode operation of the proposed LNA as described in the previous chapter. The function of M_{sw4} is controlling the peak gain for both of mode-band operation. If M_{sw4} is switched-on, the peak gain is determined by parallel connection between on-board inductor (8.2 nH) and L_d. Considering parasitic capacitances and resistances of switches, the size of $M_{sw1}, M_{sw2}, M_{sw3}$, and M_{sw4} are $W/L = 20\mu, 60\mu, 10\mu, 25\mu/0.18\mu$, respectively.

It is well known that M_{11} and M_{22} can offer a better reverse isolation as well as reducing the effect of $M_1^{'}$ and M_2's C_{gd}. The total node capacitance at the drain ofM_2 resonating with inductance L_d increase gain at the center frequency and provide an additional level of highly desirable band pass filtering, simultaneously [16]. For better isolation, the size of M_{11} and M_{22} are a half of the M_1 andM_2 in this work.

Transistors M_b and M_1 form a current mirror and minimize the power overhead of the bias circuit, its width is only in a small fraction of M_1. R_{b1} and

‘s adjust current through . Therefore, is chosen large enough that its equivalent noise current becomes small enough to be ignored [16]. In this work, both value of and are 1kΩ.

As shown in Fig. 3.1.1, the blocking capacitor is required to act as a perfect short circuit at all signal frequencies [33]. If the signal frequency decreases, the impedance of this capacitor will increase and its effectiveness as a coupling capacitor will be correspondingly reduced. In addition, and are bypass capacitor required to provide very small impedance (ideally, zero impedance; i.e., in effect, a short circuits) at all signal frequencies of interest [33].

3.1.3 Mathematical Analysis Verification

To verify the mathematical analysis for the input impedance (S_{11}), the voltage gain (A_v) and the noise figure (NF) in chapter 2, a curve of comparison between calculation and post-layout simulation is presented. Fig. 3.1.6 shows the calculationS_{11} of the proposed LNA using equations 2.2.16 with following parameters: , , , , , and . The S_{11} from the post-layout simulation is also shown in Fig. 3.1.6 for comparison. The result showed that the calculated S_{11} has a similar result with apost-layout simulation.

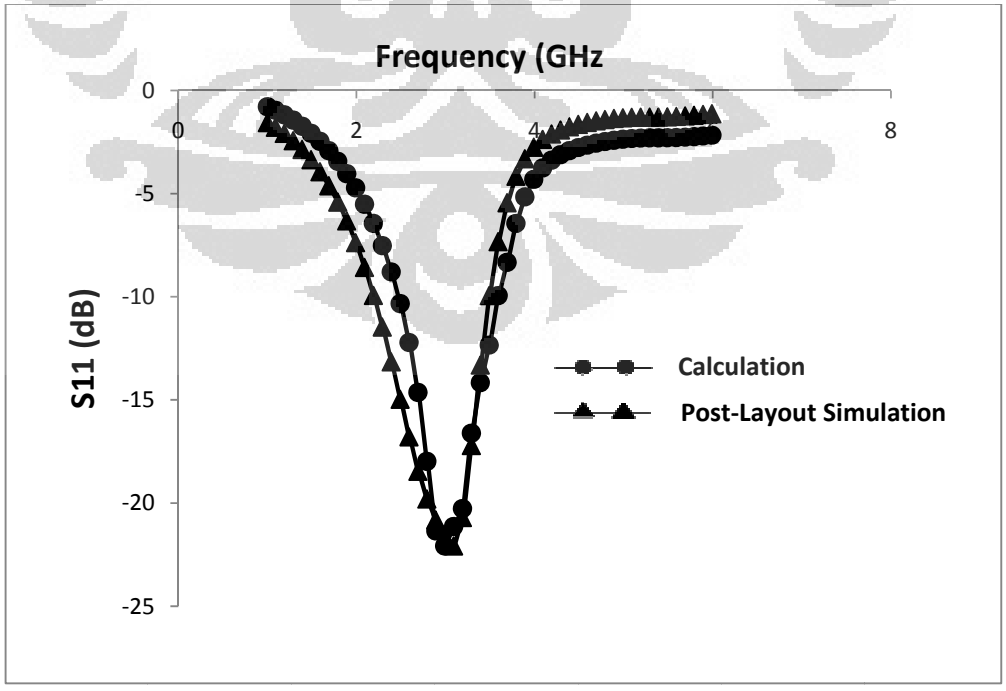


Fig. 3.1.6 S_{11} comparison for calculation and post-layout simulation

Fig. 3.1.7 represents A_v calculation by recalling 2.2.48 combined with real value design parameters from real simulation. The parameters:
and complete the following parameters shown previously. The A_v from post-layout simulation is also shown in Fig. 3.1.7 for comparison. The result shows that the peak of calculated A_v for the high-band mode lies on the frequency of interest (3.3 ~ 3.4 GHz) similar with the post-layout simulation. However, as shown in Fig. 3.1.6 and Fig 3.1.7, the sight difference between the calculation and post-layout simulation mode is the bandwidth. In post-layout simulation,the uncountable parasitics of the inductor decreases the Q [12]. Since the fractional -3-dB bandwidth of S_{11} and S_{21} in inductive source degeneration topology is inversely proportional to its Q-factor [24, 34], the bandwidth of S_{11} and A_v in the post-layout simulation is wider than in the calculation.

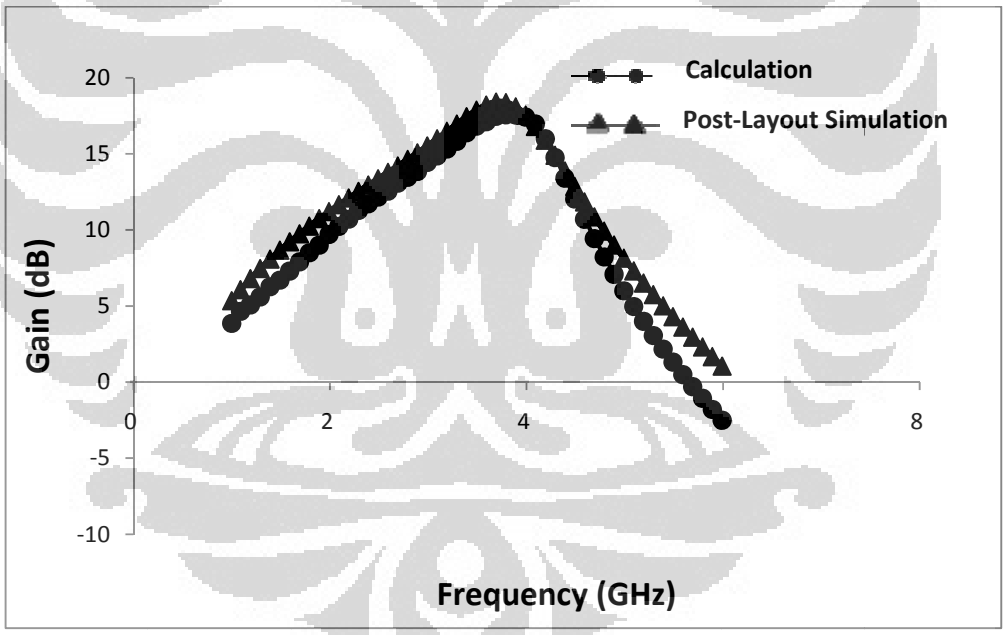


Fig. 3.1.7 A_v simulation comparison for calculation and post-layout simulation

Fig. 3.1.8 shows a noise figure performance of the proposed LNA by calculation in 2.2.64 with the following parameters: , , , , and . The contribution of and for 0.18- technology have been plotted in previous work [25] and [31], respectively. The noise figure from post-layout simulation is also shown in Fig. 3.1.8 for comparison. As can be seen, the noise figure curve reaches minimum

peak in the frequency of interest (3.3 ~ 3.4 GHz) similar with the real simulation.

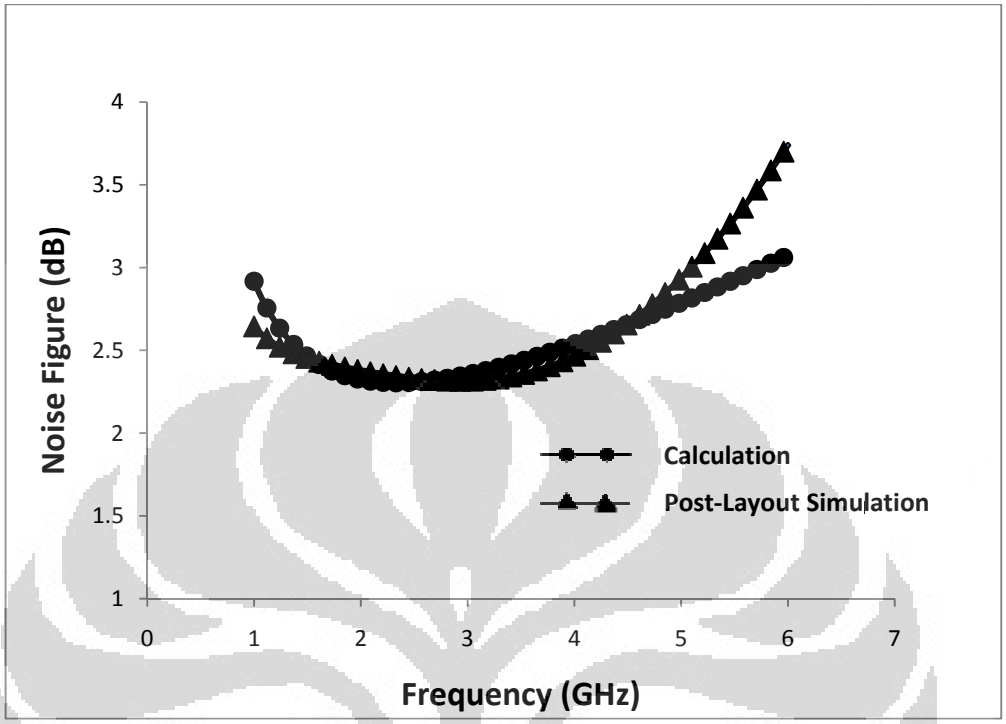


Fig. 3.1.8 Noise figure comparison for calculation and post-layout simulation

3.2 Pre-layout Circuit Simulations

3.2.1 Input Return Loss (S_{11})

The pre-layout simulation is performed by considering all the parasitic for an on-board measurement. The simulation using typical condition at room temperature of input return loss (S_{11}) is shown in the Fig. 3.2.1.1. When the switch voltage (*Vsw*) is changed from 0 V to 1.5 V, S_{11} will be shifted from lower to higher band (2.3 GHz to 3.3 GHz). The narrow band matching is achieved by the previously explanation in chapter 2. As shown in Fig. 3.2.1.1, the S_{11} is below -29 dB and -21 dB for low-band and high-band mode, respectively.

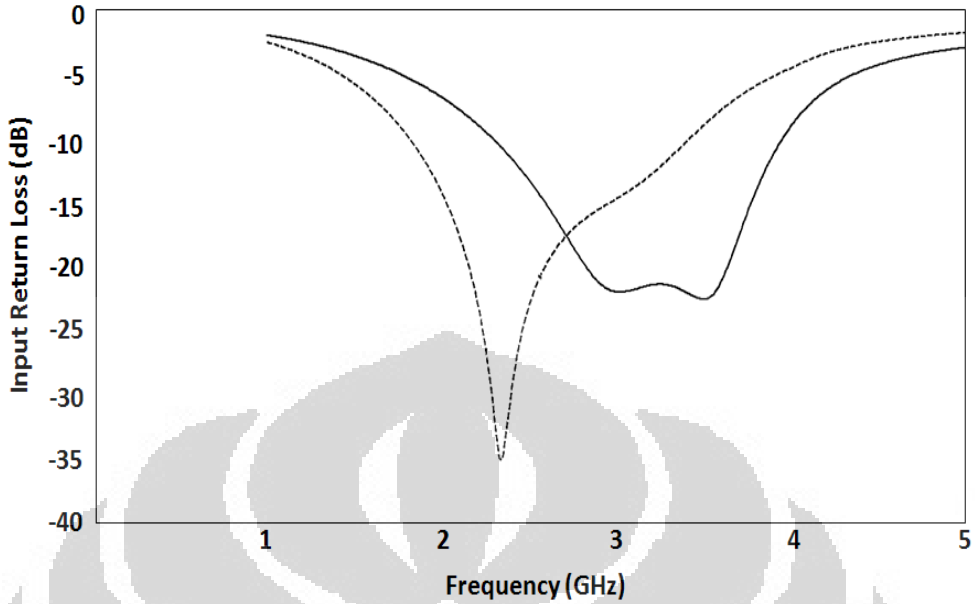


Fig. 3.2.1.1 Pre-layout simulated input return loss (S_{11}) of the proposed LNA in typical condition

By using FF corner model library at 0°C and SS corner model library at 80°Cin pre-layout simulation, the S_{11} curve is shown in Fig. 3.2.1.2. The S_{11} for low-band and high-band mode simulated in FF corner are below -32 dB and -21 dB, otherwise for SS corner are below -24 dB and -20 dB, respectively.

Moreover, the S_{11} curves for variation of VDD (± 10% from 1.5 V) are shown in Fig. 3.2.1.3. Based on the variations, the values of S_{11} are below -25 dB and -20 dB for low-band and high-band mode, respectively.

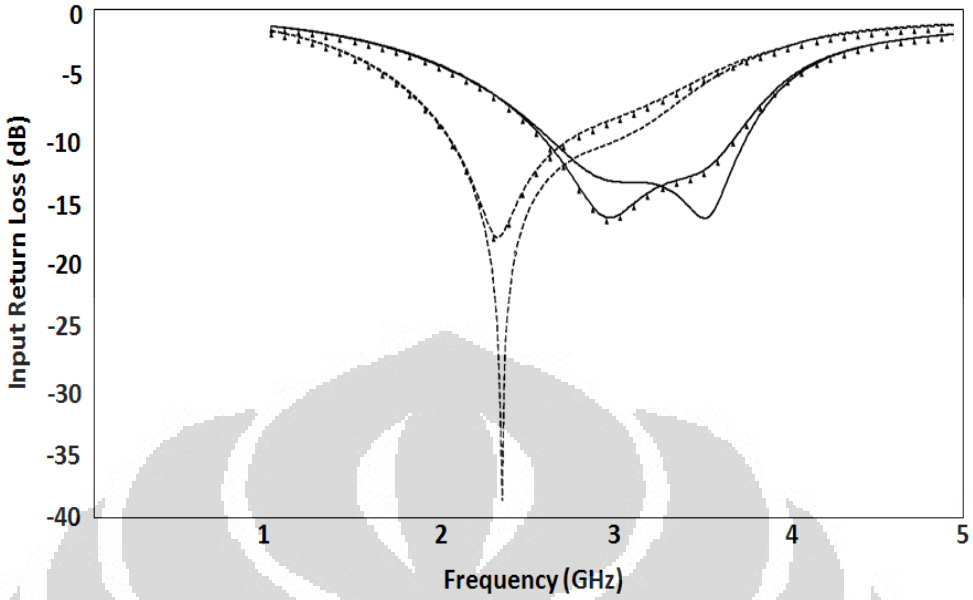


Fig. 3.2.1.2 Pre-layout simulated input return loss (S_{11}) of the proposed LNA in SS and FF corners

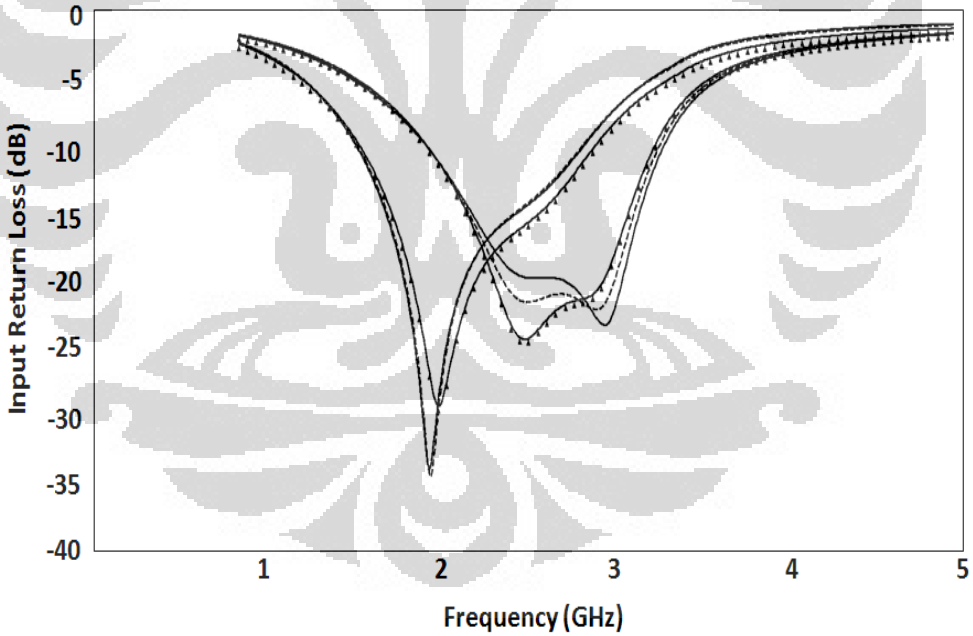


Fig. 3.2.1.3 Pre-layout simulated input return loss (S_{11}) of the proposed LNA (VDD variation)

3.2.2 Gain (S_{21})

The pre-layout simulated gain (S_{21}) of the proposed LNA in typical condition

at room temperature is shown in the Fig. 3.2.2.1. The peak S_{21} for the low-band mode tends to be constant with 1 dB variation from 2.3 GHz to 2.4 GHz, while the peak S_{21} for the high-band mode located at 3.8 GHz. The S_{21} for this simulation is above 18 dB and 17 dB for low-band and high-band mode, respectively.

Fig. 3.2.2.2 and Fig. 3.2.2.3 show the pre-layout simulation of S_{21} in FF-SS corner model libraries and in different VDD (± 10% from 1.5 V), respectively. The S_{21} of proposed LNA increases about 0.5 dB from typical model library in FF corner and decrease about 1 dB from typical model library in SS corner. Moreover, the pre-layout simulated S_{21} in ±10% VDD variations varies 2% from the result in typical condition.

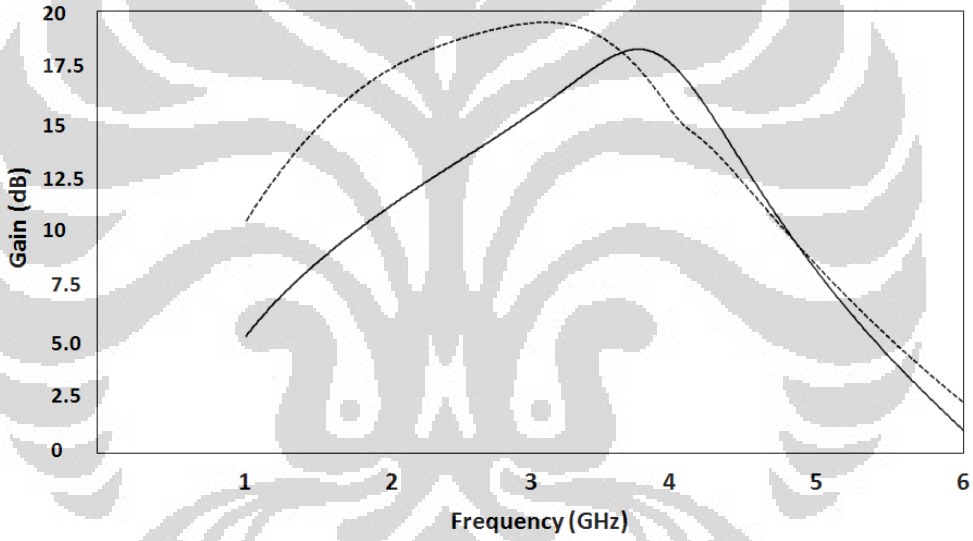


Fig 3.2.2.1 Pre-layout simulated gain (S_{21}) of the proposed LNA in typical model library

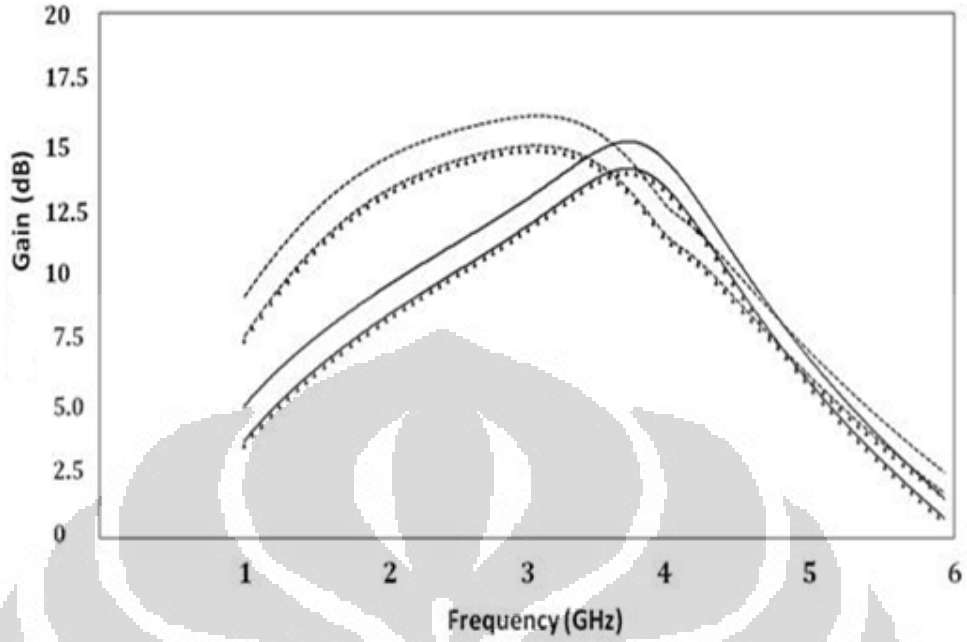


Fig. 3.2.2.2 Pre-layout simulated gain (S_{21}) of the proposed LNA in SS and FF corners

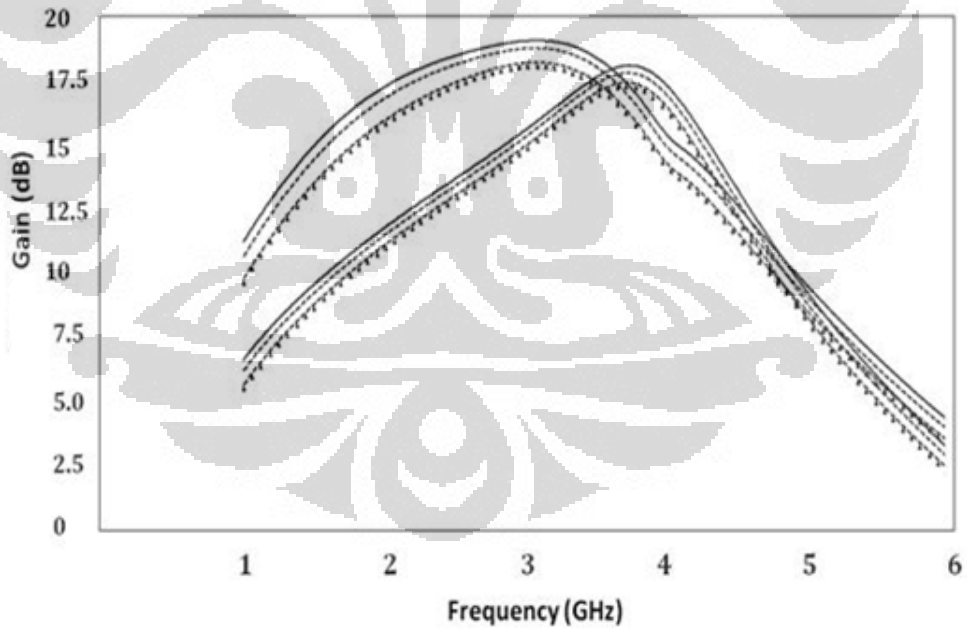


Fig. 3.2.2.3 Pre-layout simulated gain (S_{21}) of the proposed LNA (VDD variation)

The difference S_{21} performance for two mode operation of the proposed LNA is due to the difference of drain inductor used for each mode, as mentioned in sub-chapter 3.1.1.From previous explanation, since the Q-factor of drain

inductor for high-band mode is higher than for low-band mode, the S_{21} bandwidth for high-band mode is narrower than for low-mode band as shown in this simulation.

3.2.3 Stability (K_f)

Fig. 3.2.3 shows the pre-layout simulated stability factor (K_f) versus frequency of the proposed LNA. It is well known that $K_f > 1$ and $\Delta < 1$are necessary for a circuit to be unconditionally stable expressed in 3.2.3.1 and 3.2.3.2, respectively. Clearly, the proposed LNA for the both of mode bands are unconditionally stable over the 0 to 10 GHz.

$$K_f = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{22}||S_{11}|} > 1 \qquad (3.2.3.1)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} < 1 \qquad (3.2.3.2)$$

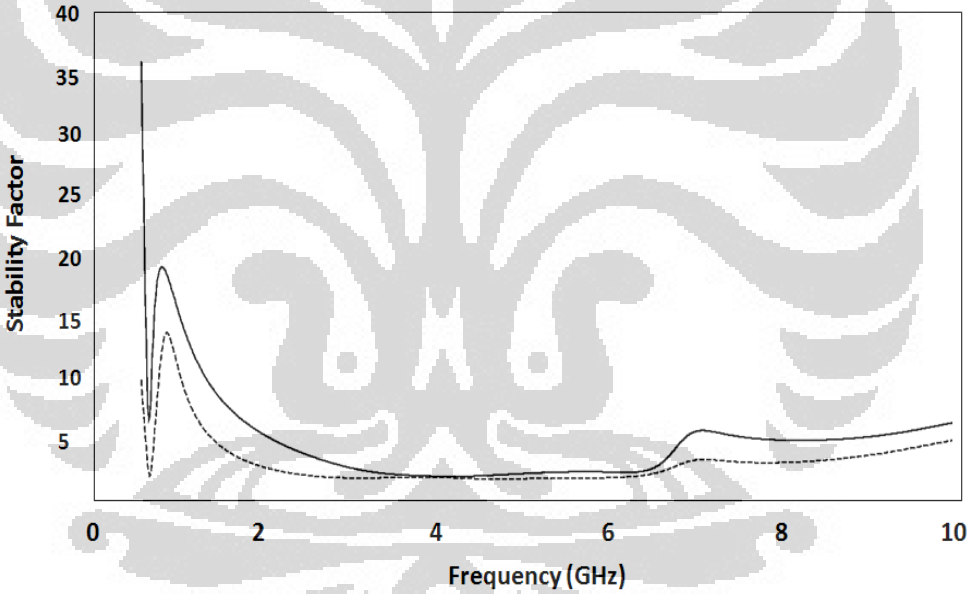


Fig 3.2.3 Pre-layout simulated stability factor (K_f) for the proposed LNA

3.2.4 Noise Figure (NF)

The noise figure (NF) of pre-layout simulation in typical condition is depicted in Fig. 3.2.4.1.The minimum NF of 1.85 dB and 2.3 dB are achieved at 1.1 GHz low-band mode and at 3 GHz for high-band mode, respectively. It also is shown in Fig. 3.2.4.1 that for both of mode-bands the NF is below 2.6 dB and 2.5 dB, respectively. Fig. 3.2.4.2 and Fig. 3.2.4.3 show the NF of the proposed LNA in different model libraries and different VDD values. As shown, in SS corner at

80°C temperature, NF degrades about 0.5 dB from typical model library result. Otherwise, 0.2 dB NF improvement can be obtained in FF corner at 0°C temperature.

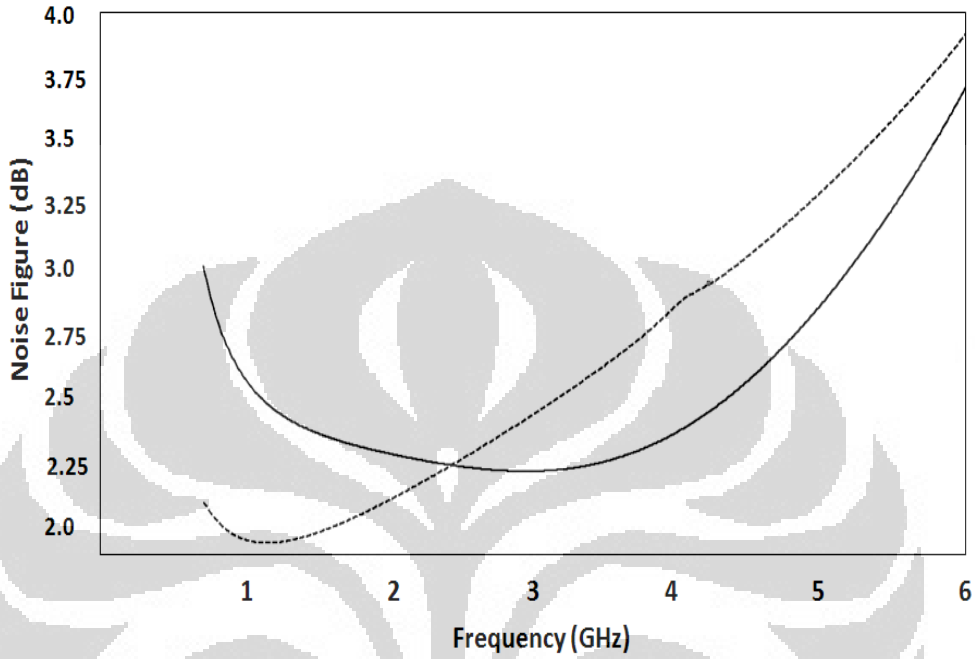


Fig 3.2.4.1 Pre-layout simulated noise figure (NF) for the proposed LNA in typical model library

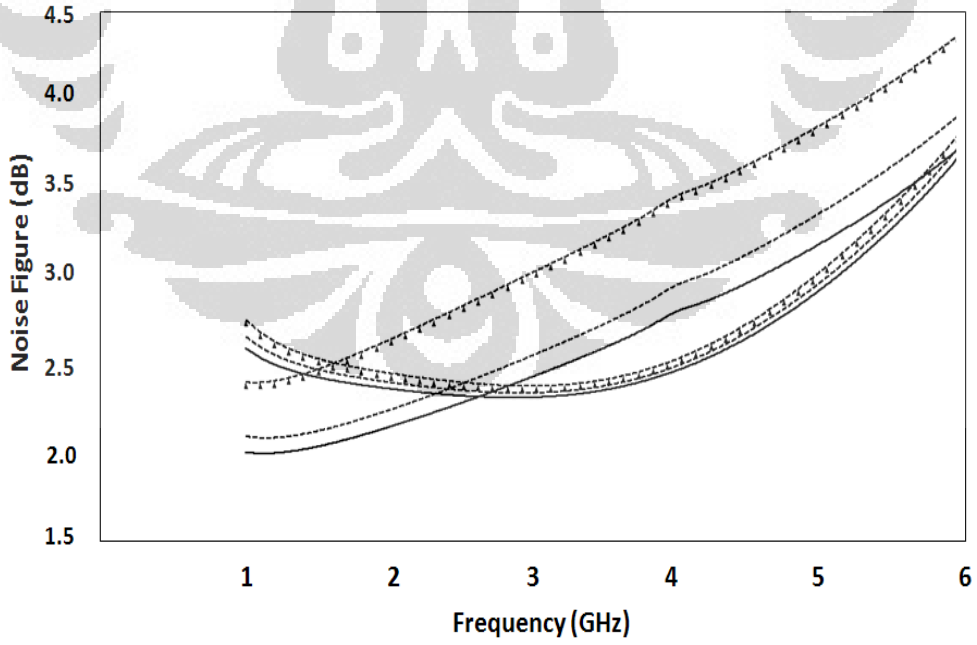


Fig 3.2.4.2 Pre-layout simulated noise figure (NF) for the proposed LNA in SS

and FF corners

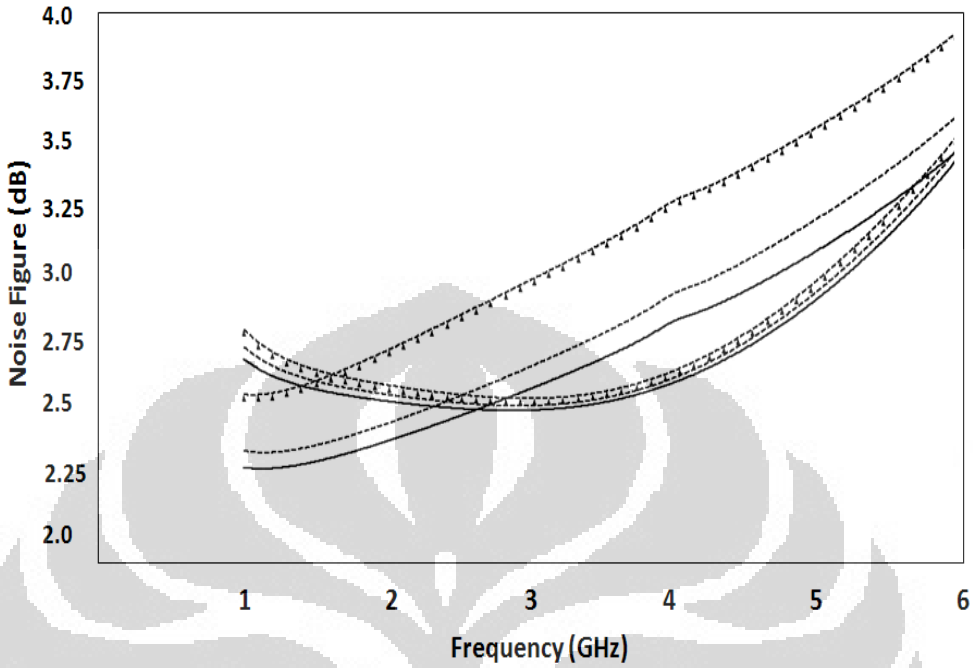


Fig 3.2.4.3 Pre-layout simulated noise figure (NF) for the proposed LNA (VDD variation)

To demonstrate the effect of VDD variation for NF, the proposed LNA is also simulated in ±10% from typical VDD as shown in Fig 3.2.4.3. According the simulation, in1.35 V, NF will degrade 0.5 dB and 0.05 dB for low-band and high-band mode, respectively. Furthermore, in 1.65 V, the NF for both of mode improves about 0.08 dB and 0.03 dB, respectively.

3.2.5 Linearity

A two-tone test is performed to evaluate IIP_3 (input third intercept points). The two-tone test for pre-layout simulation in typical condition is plotted in Fig. 3.2.5.1. It can be seen that the IIP_3 is -11.3 dBm at high-band mode frequency.

Fig. 3.2.5.2 shows the IIP_3 of low-band mode in typical condition at room temperature. It can be seen that the IIP_3 is -12.1 dBm. Meanwhile, the complete of two-tone test result based on the model library and VDD variations is depicted in Table 3.1. According to the results, the IIP_3 of proposed LNA can be improved about 1.5 dBm for low-band mode and 1 dBm for high-band mode in SS corner at 80^{o}Ctemperature, respectively. Furthermore in ±10% from typical VDD, the

proposed LNA for high-band mode has stable linearity with ±0.1 dBm variations. However, in the low-band mode the linearity varies about 0.1 to 0.4 dBm.

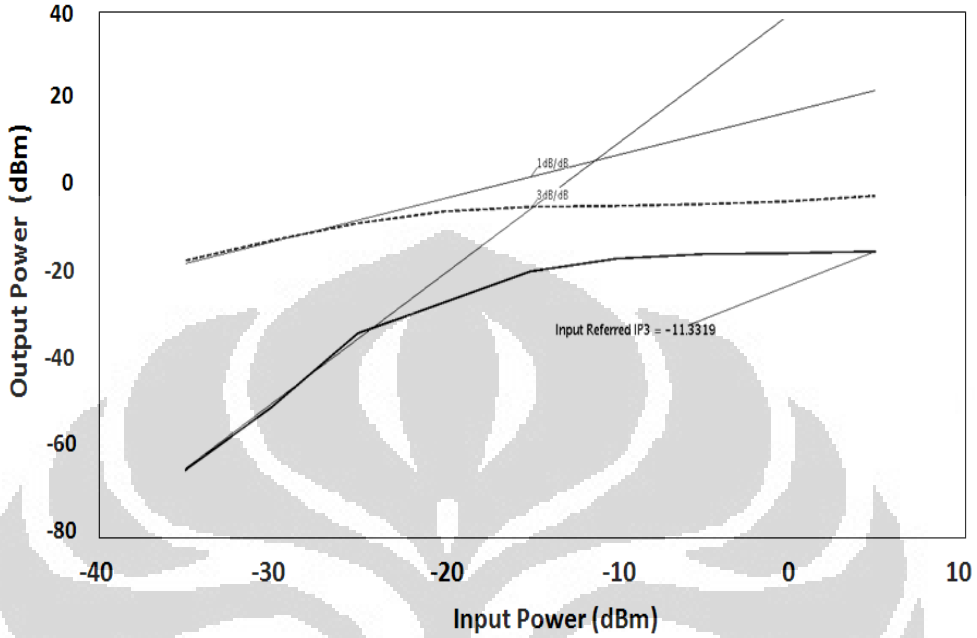


Fig. 3.2.5.1 The result of the two-tone test for IIP_3 simulation in the high-band mode of the proposed LNA

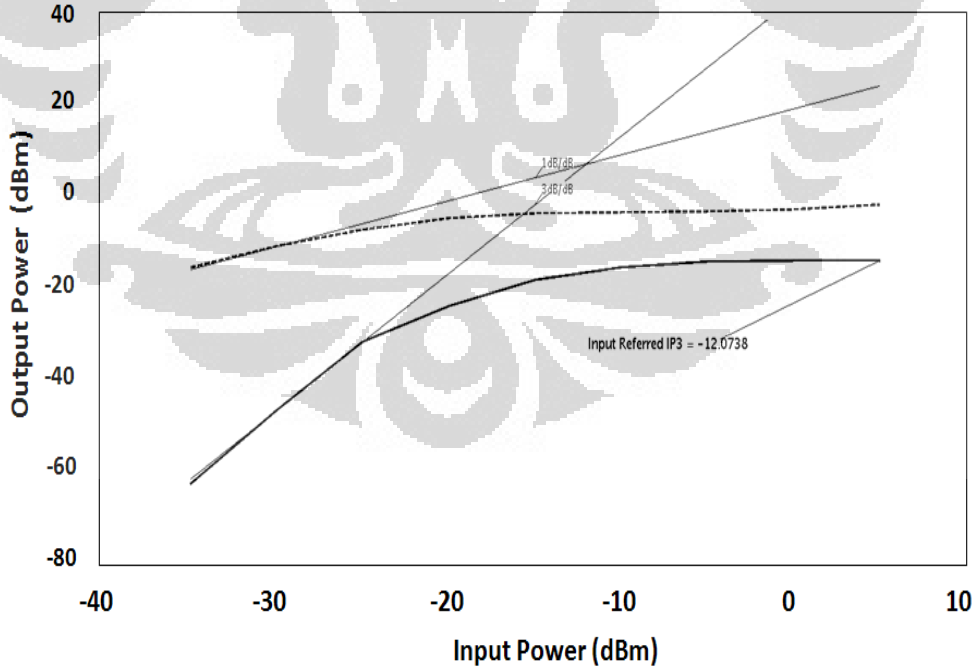


Fig 3.2.5.2 The result of the two-tone test for IIP_3 simulation in the low-band mode of the proposed LNA

Table 3.1 Two-tone test summary for IIP_3 simulation in pre-layout simulation

Item	Model Library and temperature		VDD		
	SS; 80^OC temp.	FF; 0^OC temp.	1.35 V	1.5 V	1.65 V
Low-band mode (dBm)	-10.627	-13.031	-11.62	-12.073	-12.123
High-band mode (dBm)	-10.376	-11.958	-11.42	-11.331	-11.257

Table 3.2 Performance summary of pre-layout simulation

Item (unit)	Low-band mode	High-band mode
VDD (V)	1.5 V	1.5 V
S_{11} (dB)	< -29	< -21
S_{21} (dB)	> 18.4	> 17.0
NF (dB)	< 2.6	< 2.5
IIP_3 (dBm)	-12.1	-11.3
P1dB (dBm)	-23.3	-22.1
K_f	> 1	> 1
Power Consumption (mW)	18.4	12.9

CHAPTER 4 – POST-LAYOUT SIMULATION

4.1 Post Layout Circuit

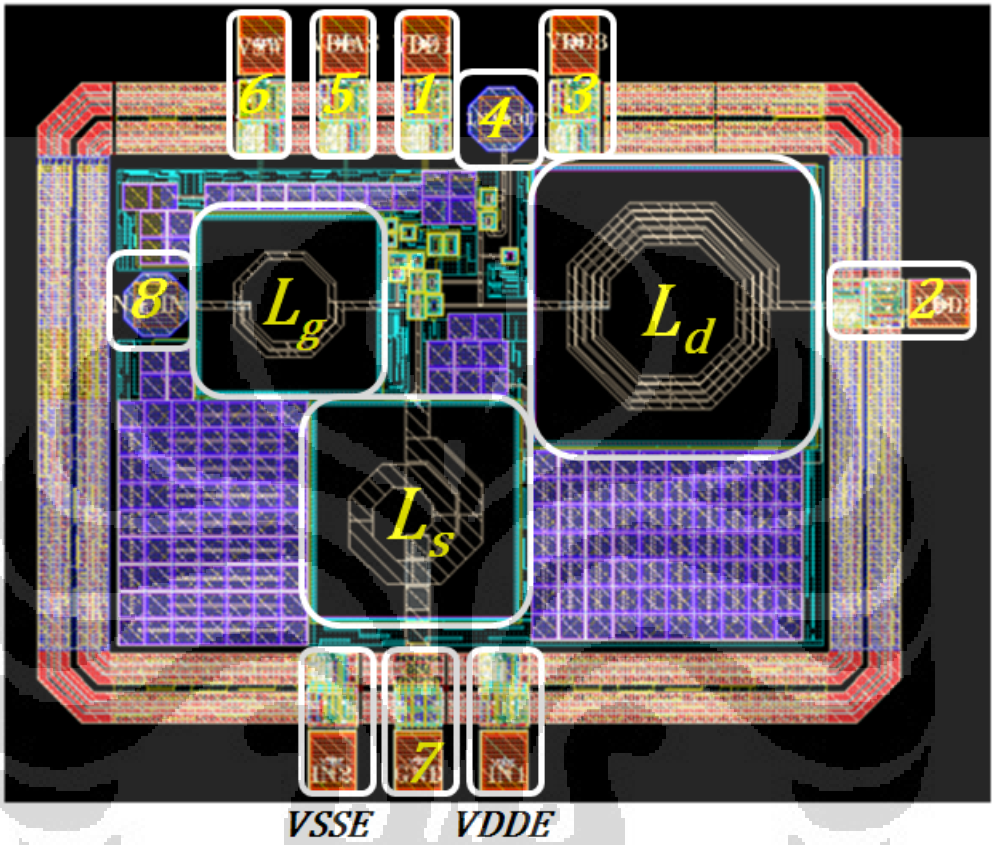


Fig. 4.1.1 Post layout for the proposed LNA circuit

The proposed of LNA in this work occupied a die area of 1.113 x 0.185 $mm^2$is shown in Fig. 4.1.1. It circuit is designed and implemented in 0.18-µm CMOS process and consists of 8 pins: VDD1, VDD2, VDD3, RF_OUT, VBIAS, VSW, GND and RF_IN shown in Fig. 3.1.1. In typical model library at room temperature (27^oC), the proposed LNA draws 10.883 mA and 7.833 mA from 1.5-V supply for low-band and high-band mode, respectively. VSSE and VDDE pins are ground and VDD pins for ESD (electrostatic discharge) protection pad.

4.2 Post-Layout Simulations

4.2.1 Input Return Loss (S_{11})

The post-layout simulation is performed by considering all the parasitic for an on-board measurement. The input return loss (S_{11}) in typical condition at room temperature is depicted in Fig. 4.2.1.1. As expected, the value of S_{11} agrees well with that of the pre-layout simulation in sec. 3.2.1. The simulated of S_{11} is below -29 dB and -13 dB for low-band and high-band mode, respectively. According this performance, the proposed LNA can be operated at both of WiMAX frequency band in Indonesia.

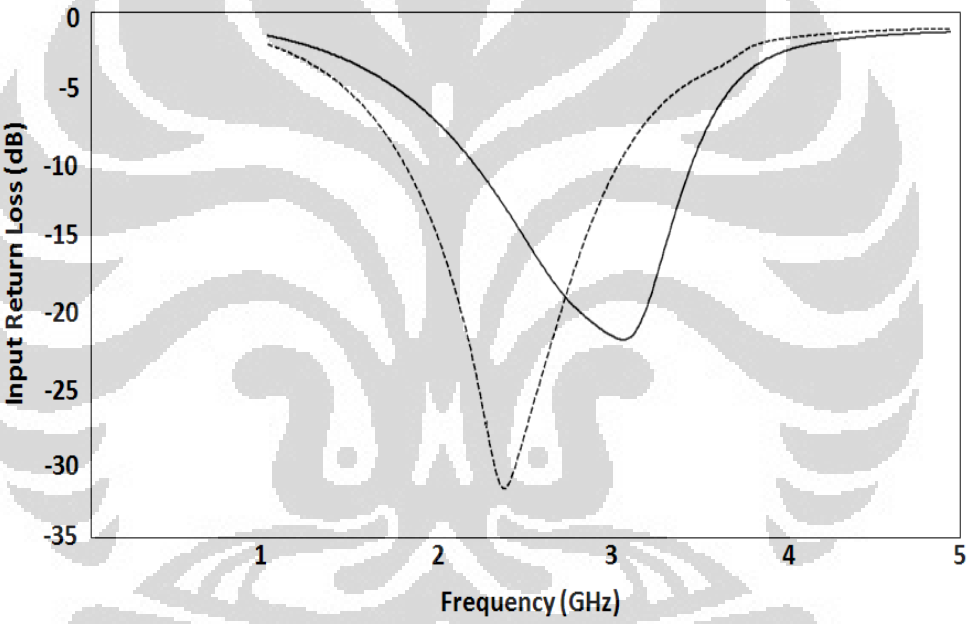


Fig. 4.2.1.1 Post-layout simulated input return loss (S_{11}) of the proposed LNA in typical condition

Furthermore, in SS and FF corners, the S_{11} remains below -10 dB over the entire band for both of mode which agrees well with the pre-layout simulation as shown in Fig. 4.2.1.2. The similar simulation result is also obtained under ±10% variation of VDD from its typical value (1.5 V) as depicted in Fig. 4.2.1.3.

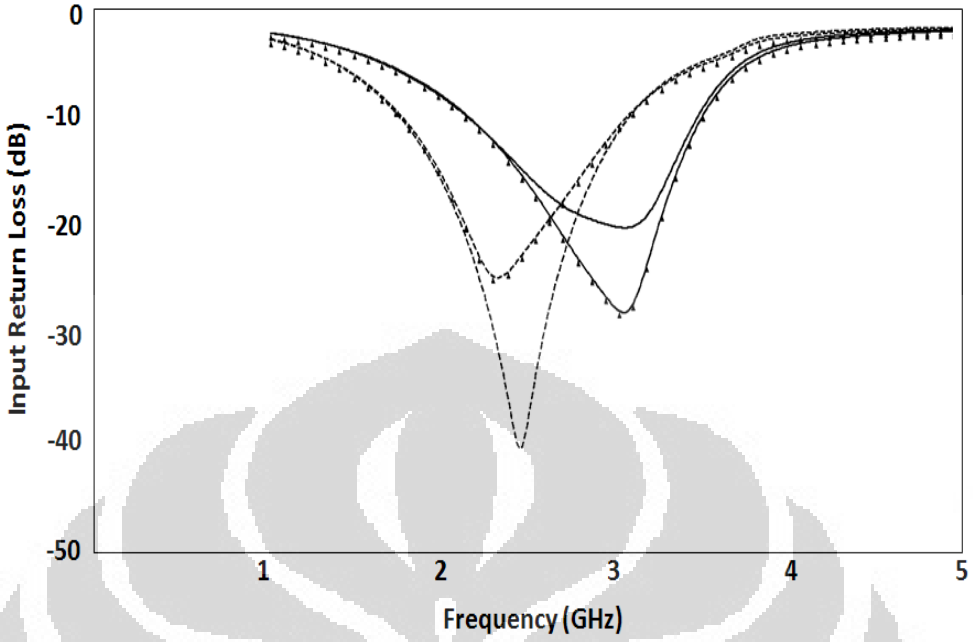


Fig. 4.2.1.2 Post-layout simulated input return loss (S_{11}) of the proposed LNA in SS and FF corners

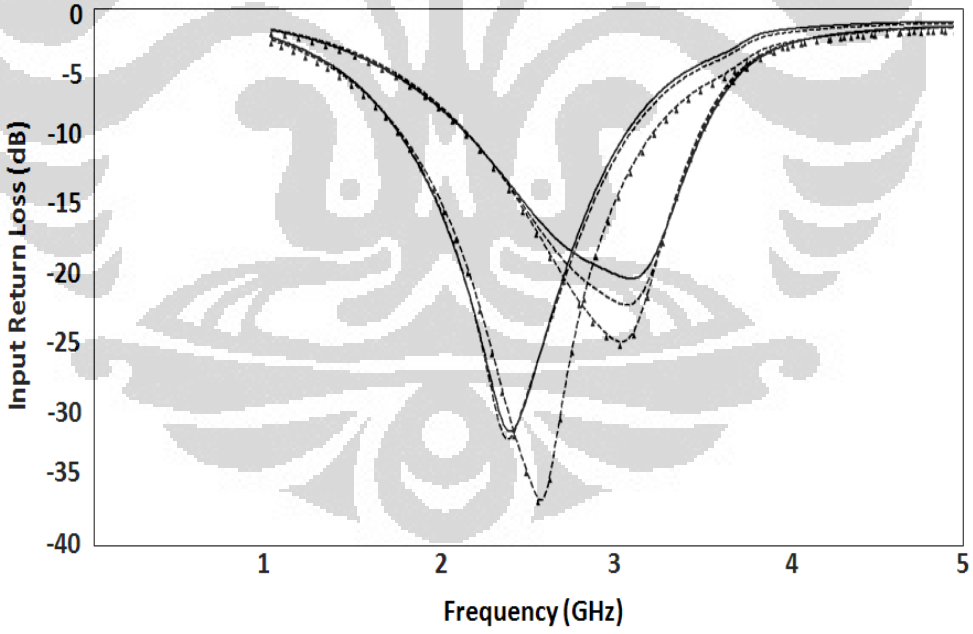


Fig. 4.2.1.3 Post-layout simulated input return loss (S_{11}) of the proposed LNA (VDD variation)

4.2.2 Gain (S_{21})

The post-layout simulated gain (S_{21}) for the proposed LNA in typical condition is 17.2~17.8 dB for low-band mode and 15.5~15.8 dB for high-band mode shown in Fig. 4.2.2.1, respectively.

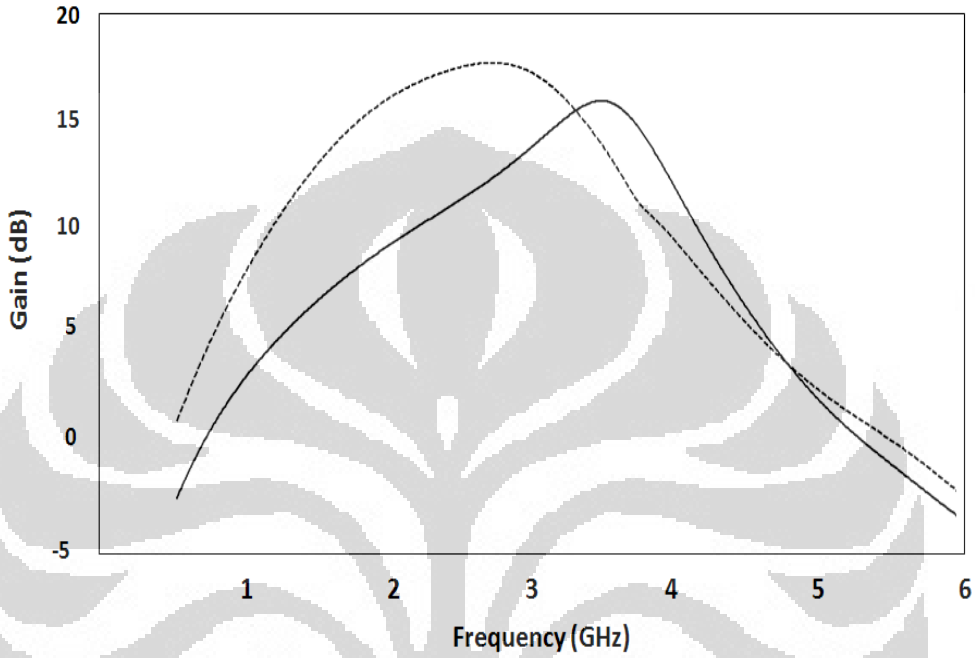


Fig 4.2.2.1 Post-layout simulated gain (S_{21}) of the proposed LNA in typical condition

Fig. 4.2.2.2 shows the post-layout simulated S_{21} inSS corner at 80°C and FF corner at 0°C, respectively. According to the simulation, S_{21} of the proposed LNA degrades about 5-6% from S_{21} in typical condition for low-band mode. Meanwhile, the S_{21} improves 3% for high-band mode. Furthermore, based on ±10% from typical VDD, the S_{21} for low-band mode are 16.12~16.40 dB and 17.64~17.86 dB in 1.35 V and 1.65 V shown in Fig. 4.2.2.3, respectively. For the similar VDD variation, the S_{21} for the proposed LNA for high-band mode are 15.12~15.47 dB and 15.79~16.18 dB in 1.35 V and 1.65 V, respectively.

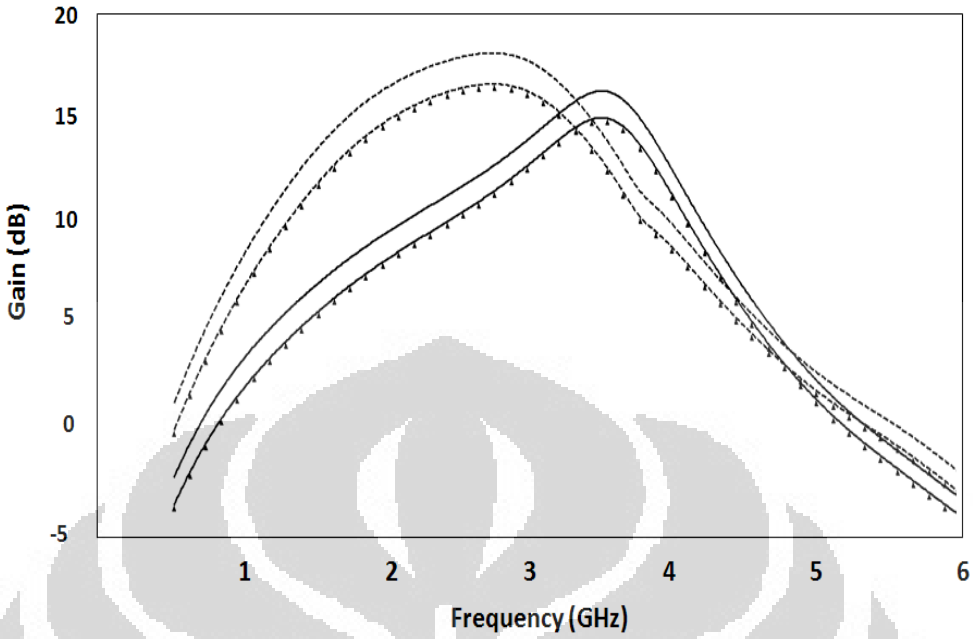


Fig 4.2.2.2 Post-layout simulated gain (S_{21}) of the proposed LNA in SS and FF corners

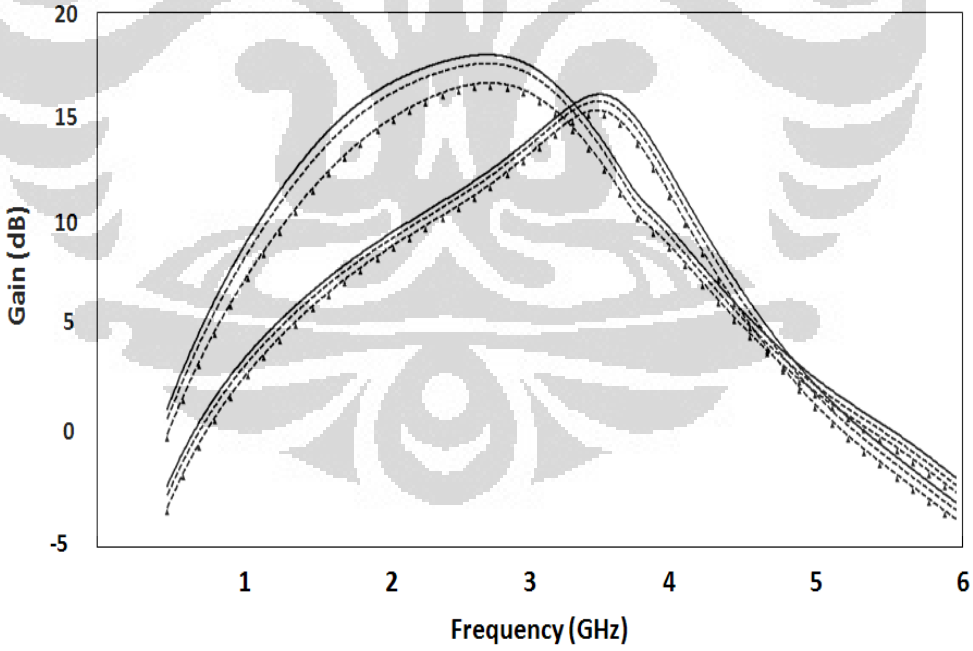


Fig. 4.2.2.3 Post-layout simulated gain (S_{21}) of the proposed LNA (VDD variation)

4.2.3 Stability (K_f)

Fig. 4.2.3.1 shows the post-layout simulated stability factor (K_f) of the proposed LNA. According to the result, the proposed of LNA for both modes are unconditionally stable over 0 to 10 GHz.

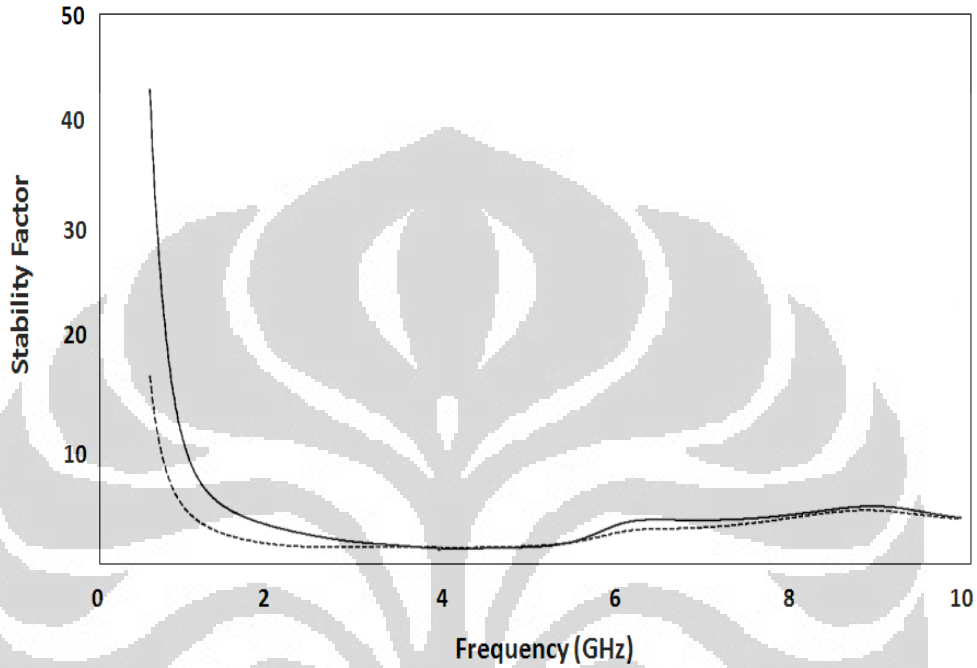


Fig. 4.2.3.1 Post-layout simulated stability factor (K_f) for the proposed LNA

4.2.4 Noise Figure (NF)

The post-layout simulated noise figure (NF) for the proposed LNA in typical condition is shown in Fig. 4.2.4.1. The NF of 2.67~2.7 dB can be achieved for low-band mode and 2.52~2.54 dB for high-band mode shown in the Fig. 4.2.4.1.

In addition, the NF can improve about 0.25 dB and 0.19 dB in FF corner for low-band mode and high-band mode shown in Fig.4.2.4.2, respectively. Otherwise, the NF degrades about 17.97% for low-band mode and 17.06% for high-band mode as depicted in that figure.

Fig. 4.2.4.3 shows the NF of the proposed LNA in ±10% VDD from typical value. As depicted in the figure, the NF varies about 0.31 dB for low-band mode while in high-band mode varies only about 0.04 dB.

Compared with the pre-layout simulation results, the post-layout simulated of NF in typical condition degrades about 15.99% for low-band mode and 8.1% for high-band mode, respectively.

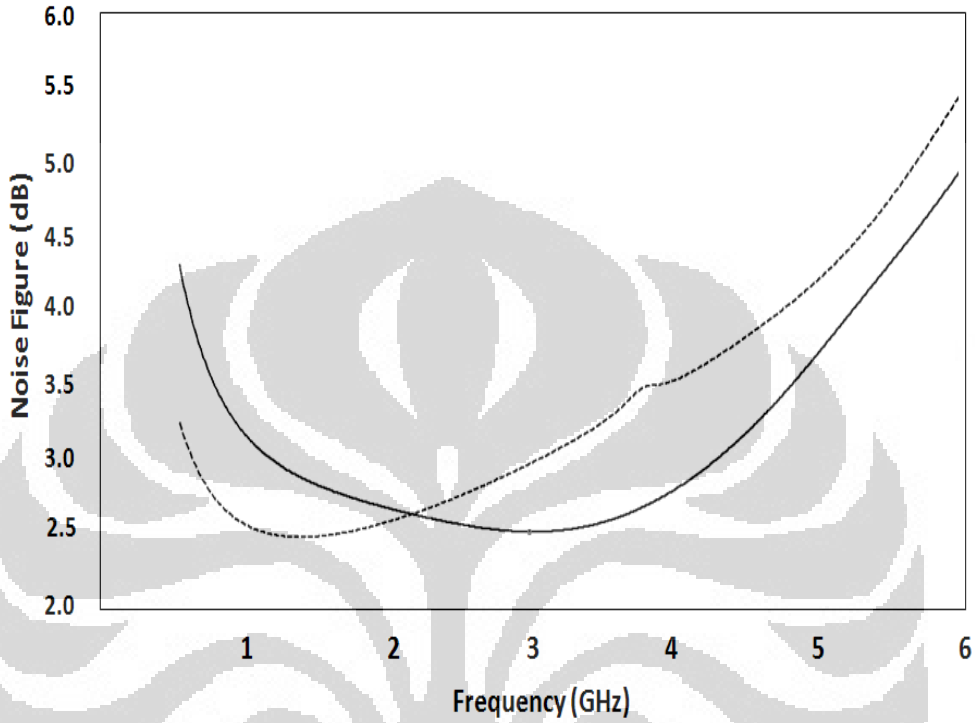


Fig 4.2.4.1 Post-layout simulated noise figure (NF) of the proposed LNA in typical condition

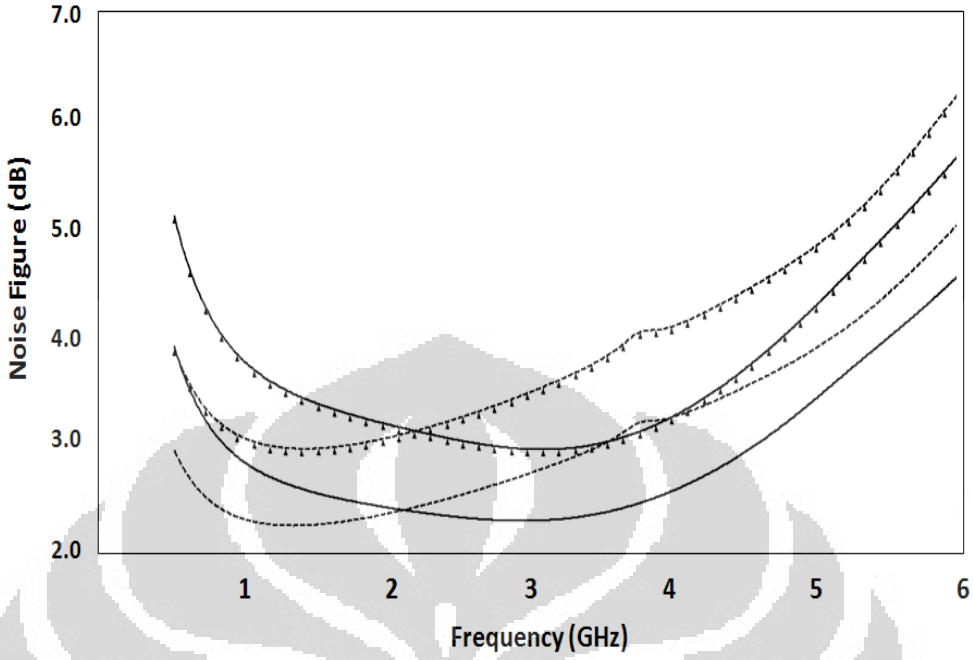


Fig 4.2.4.2 Post-layout simulated noise figure (NF) of the proposed LNA in SS and FF corners

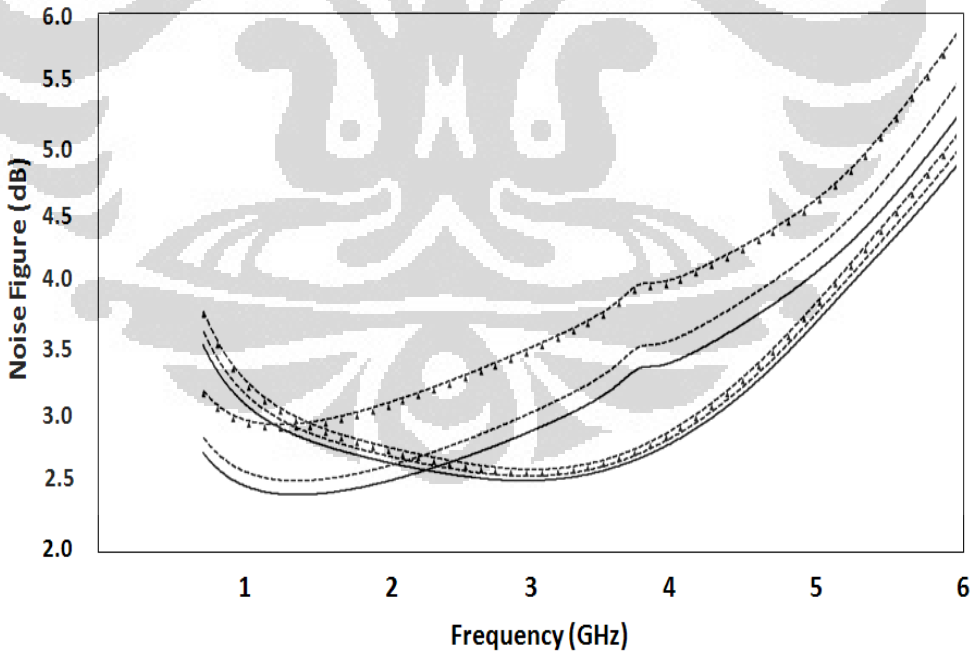


Fig. 4.2.4.3 Post-layout simulated noise figure (NF) of the proposed LNA (VDD variation)

4.2.5 Linearity

Similar with the previous chapter, a two-tone testis used to simulate linearity of the proposed LNA. The post simulated IIP_3 and P1dB for low-band mode are shown in Fig. 4.2.5.1 and Fig. 4.2.5.2, respectively. According to the figure, the IIP_3 and P1dB of the proposed LNA achieves -13.4 dBm and -24.2 dBm at low-band mode, respectively. Compared with pre-layout simulation, the IIP_3 and the P1dB for low-band mode degrade about 1.3 dBm and 0.9 dBm, respectively.

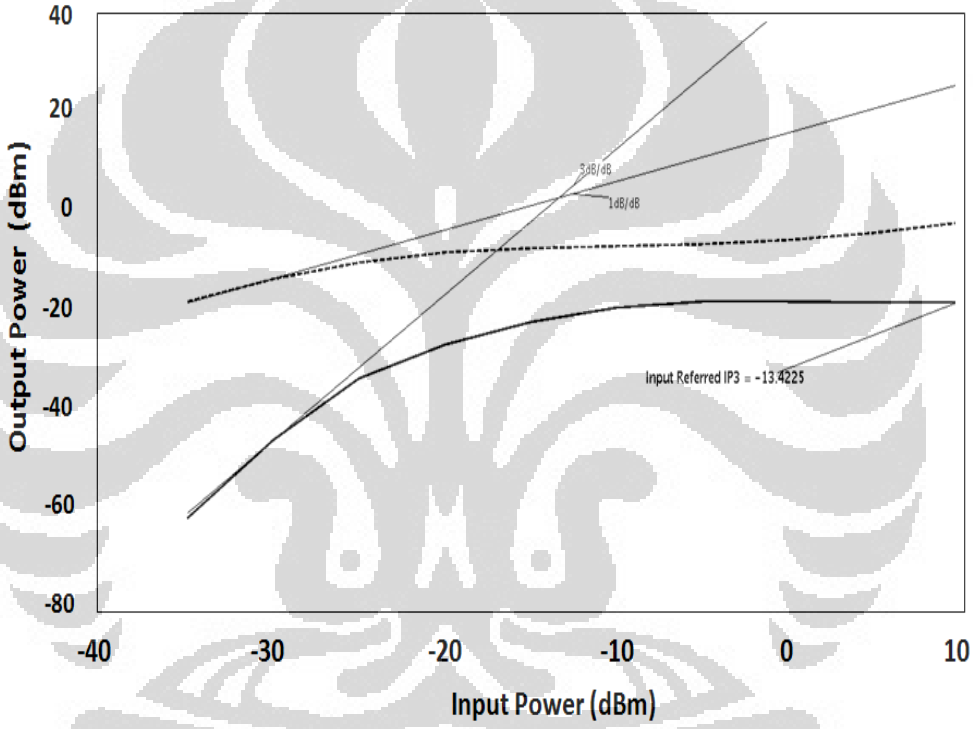


Fig 4.2.5.1 The result of the two-tone test for IIP_3 simulation in the low-band mode of the proposed LNA

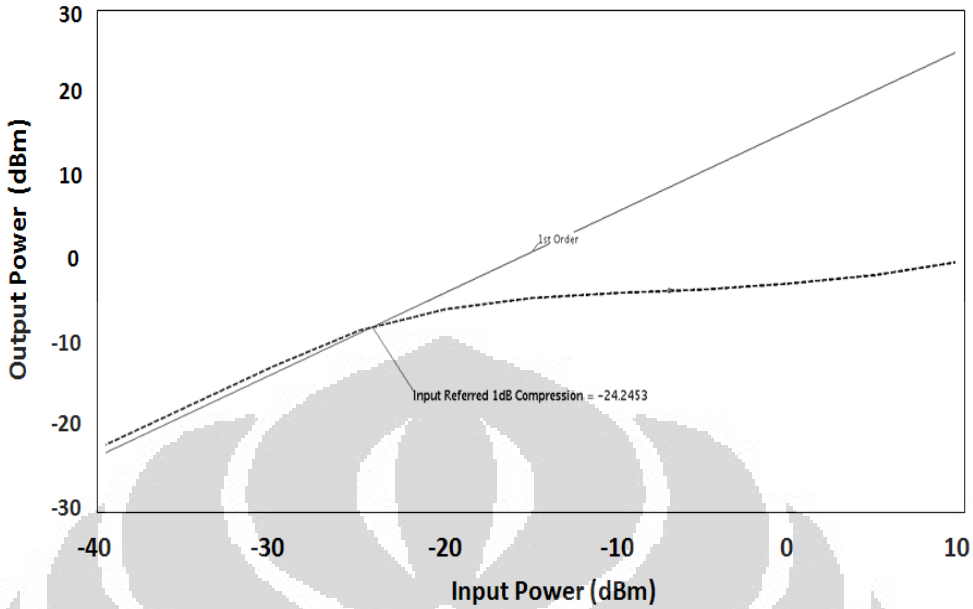


Fig 4.2.5.2 The result of P1dB simulation in the high-band mode of the proposed LNA

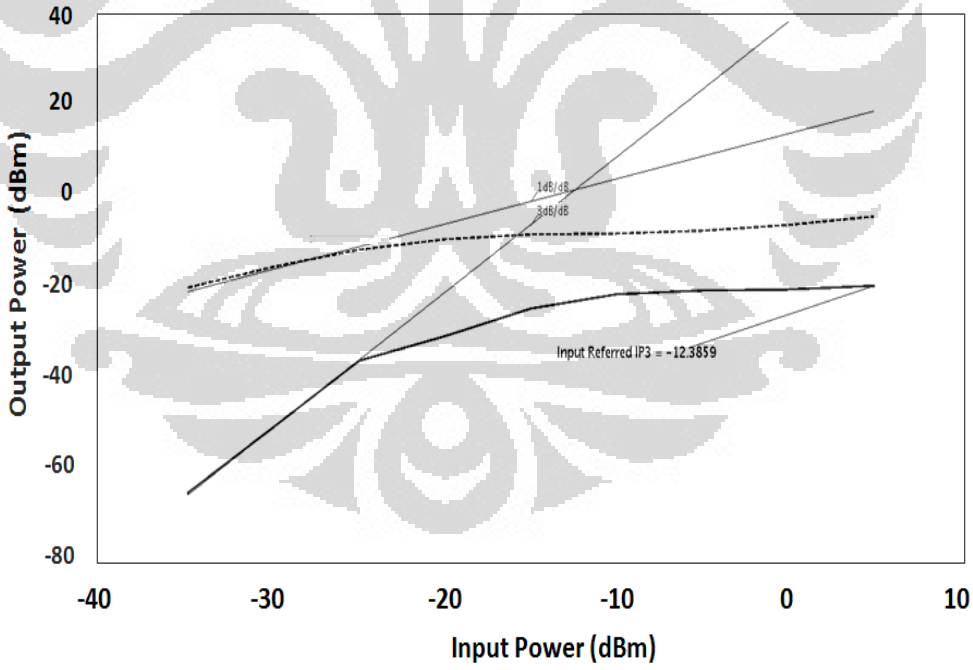


Fig 4.2.5.3 The result of the two-tone test for IIP_3 simulation in the high-band mode of the proposed LNA

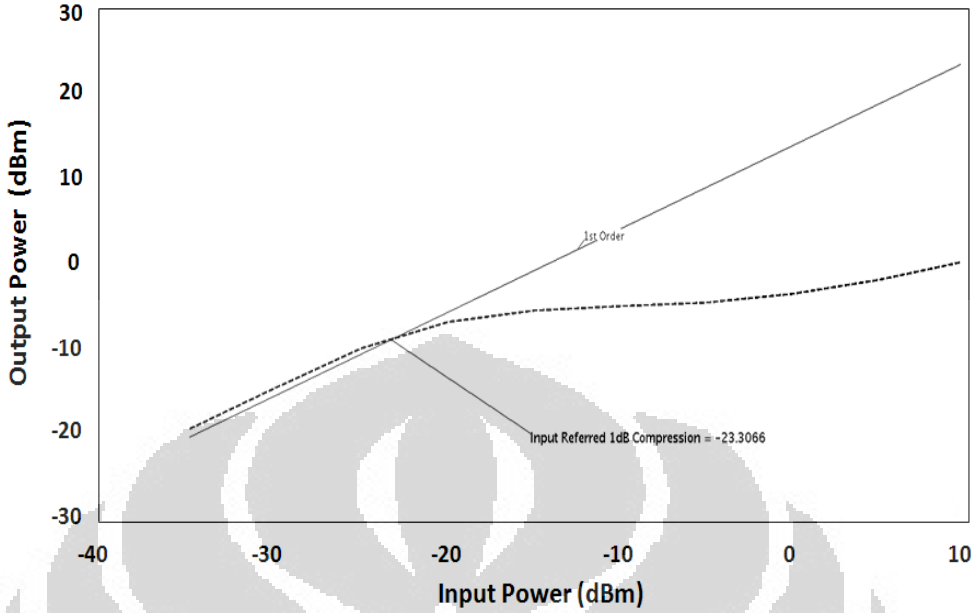


Fig. 4.2.5.4 The result of P1dB simulation in the low-band mode of the proposed LNA

Fig. 4.2.5.3 and Fig. 4.2.5.4 show the linearity performance of the proposed LNA in high-band mode. As depicted in the figure, the IIP_3 and the P1dB for the high-band mode are -12.4 dBm and -23.3 dBm, respectively. Compared with pre-layout simulation, the IIP_3 and the P1dB for high-band mode degrade about 1.1 dBm and 1.2 dBm, respectively.

For the summary, a two-tone test results in post-layout simulation based variation on corner model libraries and ±10% VDD are shown in Table 4.1. As depicted in the table, the IIP_3 increases 11.67% and 6% from typical condition in SS corner for low-band and high-band mode, respectively. However, the IIP_3 degrades about 7.17% and 8.25%from typical condition in FF corner for low-band mode and high-band mode, respectively. Furthermore, based on VDD variation, the IIP_3 varies about 0.55 dBm and 0.14 dB for low-band mode and for high-band, respectively.

Table 4.1 Two-tone test summary for IIP_3 simulation in post-layout simulation

Item	Model Library and temperature		VDD		
	SS 80^{O}C temp.	FF 0^{O}C temp.	1.35 V	1.5 V	1.65 V
Low-band mode (dBm)	-11.855	-14.383	-12.591	-13.422	-13.685
High-band mode (dBm)	-11.697	-13.4109	-12.1567	-12.385	-12.444

Table 4.2 Performance summary of post-layout simulation

Item (unit)	Low-band mode	High-band mode
VDD (V)	1.5 V	1.5 V
S_{11} (dB)	<-29	<-13
S_{21} (dB)	> 17	> 15.5
NF (dB)	< 2.71	< 2.54
IIP_3 (dBm)	-13.4	-12.3
P1dB (dBm)	-24.2	-23.3
Stability Factor (K_f)	> 1	> 1
Power Consumption (mW)	16.32	11.75

Table 4.2 and Table 4.3 show the performance summary of post-layout simulation and the comparison of the proposed LNA with other works, respectively.

Table 4.3 Simulation results of the proposed LNA and other works

Ref.	This Work		[35]	[36]	[37]	[38]
	2.3 GHz	3.3 GHz				
Frequency (GHz)	2.3~2.4	3.3~3.4	2.4	0.9	0.9	0.96
S_{11}(dB)	-29.1~-32	-12.9~-16.8	-20	-11	-14	< -10
S_{21}(dB)	17.2~17.8	15.5~15.8	13	17.5	17	13
NF(dB)	2.67~2.71	2.52~2.54	3.6	2.05	3.4	3.6

IIP_3(dBm)	-13.4 (@2.3GHz)	-12.3 (@3.3GHz)	-3	-6	-5.1	-10
P1dB(dBm)	-24.2 (@2.3GHz)	-23.3 (@3.3GHz)	-	-	-	-18
VDD (V)	1.5	1.5	1.5	2.7	2.3	1.2
Power Cons.(mW)	16.3	11.75	7.2	21.6	12.8	0.72
Chip Area (mm^2)	0.9	0.9	0.56	-	0.35	2.6

Furthermore, to compare overall performance of the proposed LNA, the FOM formulas [39][41][42][31] are used as shown in Table 4.4.

$$\mathrm{FOM^1(mW^{-1})} = \frac{\mathrm{Gain[abs]}}{(\mathrm{NF}-1)[\mathrm{abs}].\,\mathrm{P_{DC}[mW]}} \quad (4.2.1)$$

$$\mathrm{FOM^2(-)} = \frac{\mathrm{Gain[abs]}.\,\mathrm{IIP_3[mW]}.\,\mathrm{f_c[GHz]}}{(\mathrm{NF}-1)[\mathrm{abs}].\,\mathrm{P_{DC}[mW]}} \quad (4.2.2)$$

$$\mathrm{FOM^3} = 10.\log_{10}\left(100.\frac{\mathrm{Gain[abs]}.\,\mathrm{IIP_3[mW]}}{(\mathrm{F}-1)[\mathrm{abs}].\,\mathrm{P_{DC}[mW]}}\right) + 10.\log_{10}\left(\frac{\mathrm{f_o}}{1\mathrm{GHz}}\right) \quad (4.2.2)$$

Table 4.4 Summary Figure of Merit (FOM) of the proposed LNA and other works

Ref.	This Work		[35]	[36]	[37]	[38]
	2.3 GHz	3.3 GHz				
Gain/P_{DC}	1.068	1.352	1.805	0.801	1.319	1.805
FOM^1	0.639	0.889	0.694	0.771	0.549	0.601
FOM^2	0.079	0.172	0.062	0.173	0.156	0.051
FOM^3	16.78	19.03	12.86	19.41	19.73	11.95

Summary of FOMs in Table 4.4 indicates that the proposed LNA in this work can compete with the other published and implemented LNA based on on-board measurement in terms of S_{21}, NF, IIP_3, power consumption and frequency of operation.

4.3 Measurement Method

Fig. 4.3.1 is proposed PCB board for the proposed LNA measurements. This board is designed by Allegro PCB Design Expert.

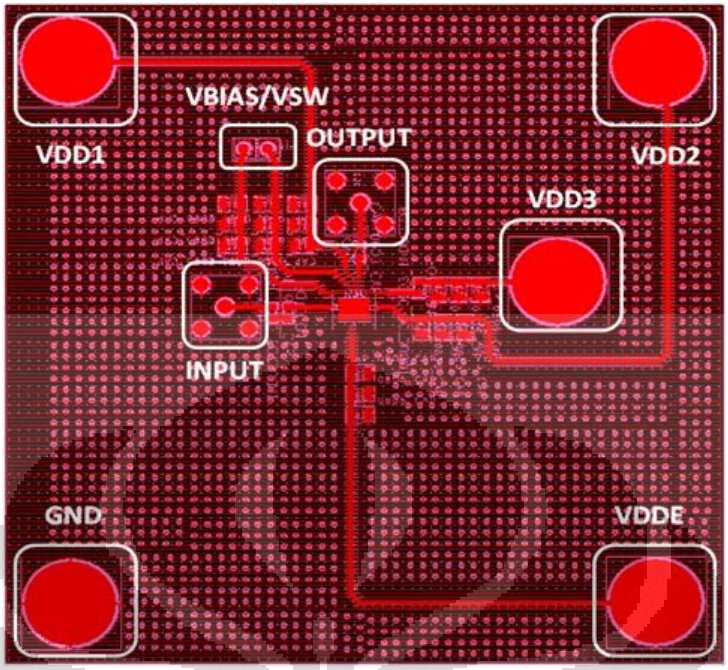


Fig. 4.3.1 PCB board for chip measurements

As depicted in Fig. 3.1.1, the PCB board consists of 10 pins, including VDDE and VSSE. VSSE is connected to GND pad, while VDDE is connected to VDDE pad to provide VDD for ESD chip protection.

Fig. 4.3.2 and Fig. 4.3.3 show measurement setups for S_{11}, S_{21}, IIP_3, and P1dB on-board measurements, respectively. As shown in the figure, in order to measure S_{11} and S_{21}, the network analyzer is needed. In other hand, the signal generator is needed for providing LNA's input signal while spectrum analyzer for displaying the IIP3 and P1dB results as depicted in Fig. 4.3.3.

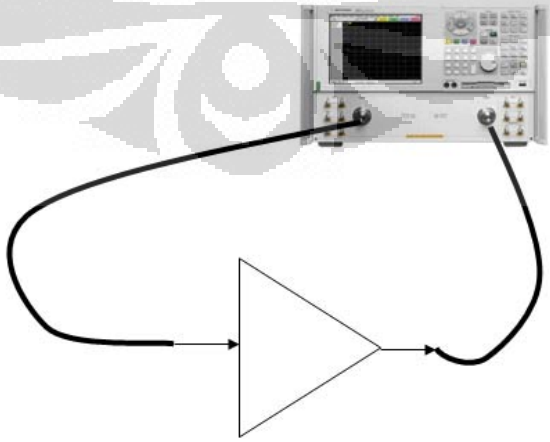


Fig. 4.3.2 Measurement setup for S_{11}, S_{21} test

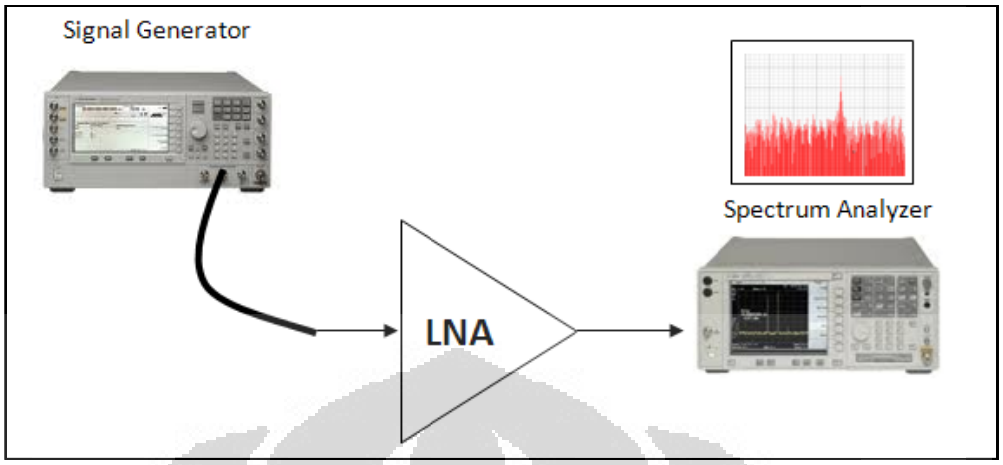


Fig. 4.3.3 Measurement setup for linearity test

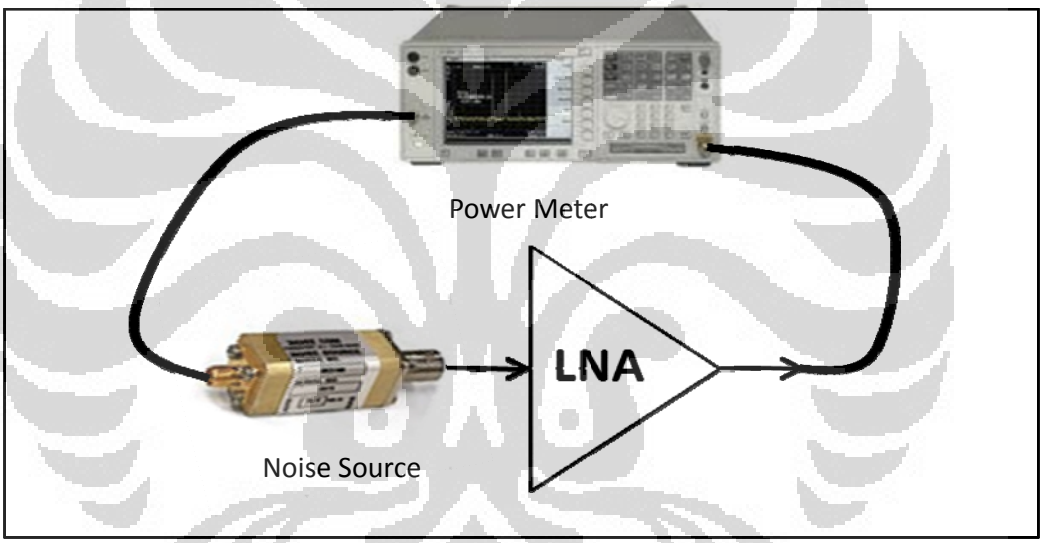


Fig. 4.3.4 Measurement setup for NF test

Furthermore, Fig. 4.3.4 shows a measurement setup for common method of NF test. This method is known as Y Factor Method with using a spectrum analyzer and noise source. Calibrated broadband noise source that contains two temperature states, high temperature with a higher output of noise power and low temperature with reduced noise output, is used by this technique simultaneously. The noise source is applied to the input of the proposed LNA under test and the noise power of the proposed LNA will be measured for each of the two input noise states.

CHAPTER 5 – CONCLUSIONS

In this thesis, a 2.3/3.3 GHz dual band LNA as one of important part of front-end WiMAX receiver was successfully realized using inductive source degeneration with switchable inductor for gain controlling. In chapter 2, we have presented mathematical analysis of input impedance, newly conceived gain and noise figure equations for source inductive degeneration LNA architecture, which modifies the equations in previous works.

In chapter 3, the proposed of LNA was simulated in pre-layout simulation. At the low-band mode, pre-layout simulation results show that the S_{11} is lower than -29 dB, the S_{21} of 18.45 ~ 18.69 dB, and the NF of 2.3 ~ 2.33 dB. The IIP_3 and P1dB are -12.1 dBm and 23.3 dBm, respectively, while total power consumption is 18.4 mW at 1.5 V power supply. At high-band mode, pre-layout simulation results show the S_{11} is lower than -21 dB, the S_{21} of 17.01 ~ 17.48 dB, and the NF of 2.36 ~ 2.37 dB. The IIP_3 and P1dB are -11.3 dBm and -22.1 dBm, respectively, while total power consumption was 12.9 mW at 1.5 V power supply. These pre-simulation results also tend to be relatively stable in variations of VDD and corner library as explained.

In chapter 4, the proposed of LNA is simulated in post-layout simulation using standard 0.18-μm CMOS technology. Total chip area is 0.9 mm^2 including the test pads. By post-layout simulation, the proposed of LNA for low-band mode achieved the S_{11} of -29.11 dB ~ -32 dB, the S_{21} of 17.18 ~ 17.42 dB, and the NF of 2.67 ~ 2.71 dB. For linearity performance, the IIP_3 and P1dB are -13.4 dBm and -24.2 dBm, respectively. In low-band mode, this proposed LNA consumed only a small dc power of 16.32 mW. At high-band mode, post-simulation results show the S_{11} is -12.94 ~ -16.82 dB, the S_{21} of 15.5 ~ 15.88 dB, and the NF of 2.52 ~ 2.54 dB. Furthermore, the IIP_3 and P1dB for the high-band mode are -12.3 dBm and 23.3 dBm by consuming only 11.75 mW at 1.5 V power supply, respectively.

The main achievement of this master work is the post-layout simulation of 2.3/3.3 dual band LNA with inductive source degeneration architecture and proposed gain controlling by switchable inductor for WiMAX applications in Indonesia. The circuit realized in the 0.18-μm CMOS technology will be

fabricated and measured in on-board as explained in chapter 4. In future, because of its well-performance, this proposed LNA is very promising for dual-band frequency RFIC applications especially to support communication infrastructure development as a part of WiMAX chip in Indonesia and also in the world.

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Appendix

PRE-LAYOUT SIMULATION RESULTS

2.3~2.4 GHz Pre-Simulation in 5-Corner Libraries

Model Library	VDD (V)	2.3~2.4 GHz				
		S11 (dB)	S21(dB)	NF (dB)	Power (mW)	IIP3(dBm)
TT	1.35	-25.32 ~ -29.74	17.5 ~ 17.79	2.736 ~ 2.775	13.7421	-11.62
	1.5	-31.77 ~ -29.38	18.45 ~ 18.69	2.302 ~ 2.333	18.4129	-12.0738
	1.65	-32.27 ~ -28.59	18.85 ~ 19.07	2.197 ~ 2.226	23.7737	-12.1234
FF	1.35	-21.75 ~ -24.18	17.92 ~ 18.21	2.565 ~ 2.603	13.6207	-12.4238
	1.5	-32.79 ~ -32.78	18.97 ~ 19.2	2.081 ~ 2.11	18.3089	-13.031
	1.65	-34.56 ~ -32.5	19.34 ~ 19.55	1.984 ~ 2.011	23.6962	-13.082
SS	1.35	-29.58 ~ -34.22	16.57 ~ 16.87	3.129 ~ 3.169	13.9272	-10.333
	1.5	-26.87 ~ -24.76	17.45 ~ 17.71	2.738 ~ 2.771	18.5753	-10.6275
	1.65	-26.87 ~ -24.35	17.9 ~ 18.13	2.615 ~ 2.646	23.9031	-10.6643
FS	1.35	-25.29 ~ -29.73	17.5 ~17.79	2.737 ~ 2.775	13.7334	-11.62
	1.5	-31.87 ~ -29.42	18.45 ~ 18.69	2.302 ~ 2.333	18.4036	-12.0738
	1.65	-32.43 ~ -28.59	18.85 ~ 19.07	2.197 ~ 2.226	23.7657	-12.1234
SF	1.35	-25.29 ~ -29.74	17.5 ~ 17.79	2.737 ~ 2.775	13.7334	-11.62
	1.5	-31.79 ~ -29.42	18.45 ~ 18.69	2.302 ~ 2.333	18.4036	-12.0738
	1.65	-32.36 ~ -28.59	16.85 ~ 19.07	2.197 ~ 2.226	23.7657	-12.1234

3
.3~3.4 GHz Pre-Simulation in 5-Corner Libraries

Model Library	VDD (V)	3.3~3.4 GHz				
		S11(dB)	S21(dB)	NF(dB)	Power (mW)	IIP3(dBm)
TT	1.35	-21.93 ~ -21.64	16.64 ~ 17.12	2.368 ~2.378	9.669	-11.4263
	1.5	-21.36 ~ -21.93	17.01 ~ 17.48	2.331 ~ 2.341	12.9738	-11.3319
	1.65	-20.44 ~ -21.51	17.28 ~ 17.75	2.307 ~ 2.317	16.768	-11.2573
FF	1.35	-22.33 ~ -22.97	17.14 ~ 17.61	2.15 ~ 2.16	9.587	-12.0574
	1.5	-21.18 ~ -22.58	17.48 ~ 17.95	2.119 ~ 2.13	12.8992	-11.9582
	1.65	-19.96 ~ -21.54	17.73 ~ 18.2	2.1 ~ 2.111	16.7079	-11.8622

SS	1.35	-20.59 ~ -19.39	15.75 ~ 16.23	2.783 ~ 2.791	9.7023	-10.4797
	1.5	-20.79 ~ -20.14	16.16 ~ !6.64	2.734 ~ 2.742	13.103	-10.3763
	1.65	-20.55 ~ -20.45	16.46 ~ 16.93	2.701 ~ 2.71	16.881	-10.3065
FS	1.35	-21.93 ~ -21.64	16.64 ~ 17.12	2.368 ~ 2.378	9.669	-11.7292
	1.5	-21.36 ~ -21.93	17.28 ~ 17.75	2.331 ~ 2341	12.973	-11.6448
	1.65	-20.45 ~ -21.52	17.01 ~ 17.48	2.307 ~ 2.317	16.768	-11.5757
SF	1.35	-21.93 ~ -21.64	16.64 ~ 17.12	2.368 ~ 2.378	9.669	-11.7292
	1.5	-21.36 ~ -21.93	17.01 ~ 17.48	2.331 ~ 2.341	12.973	-11.6448
	1.65	-20.44 ~ -21.5	17.28 ~ 17.75	2.307 ~ 2.317	16.768	-11.5757

POST-LAYOUT SIMULATION RESULTS

2.3~2.4 GHz Post-Simulation in 5-Corner Libraries

Model Library	VDD (V)	2.3~2.4 GHz				
		S11 (dB)	S21(dB)	NF (dB)	Power (mW)	IIP3(dBm)
TT	1.35	-25.91 ~ -30.69	16.12 ~ 16.40	3.16 ~ 3.21	12.33	-12.2155
	1.5	-29.11 ~ -32.00	17.18 ~ 17.42	2.67 ~ 2.7)	16.325	-12.7328
	1.65	-28.42 ~ -31.54	17.64 ~ 17.86	2.55 ~ 2.59	21.302	-12.8629
FF	1.35	-21.47 ~ -23.26	16.54 ~ 16.82	2.97 ~ 3.01	12.16	-12.8005
	1.5	-29.10 ~ -36.77	17.71 ~ 17.95	2.43 ~ 2.46	16.16	-13.4109
	1.65	-27.92 ~ 32.67	18.16 ~ 18.38	2.32 ~ 2.35	20.72	-13.5983
SS	1.35	-29.67 ~ -31.29	15.21 ~ 15.50	3.58 ~3.63	12.58	-11.3087
	1.5	-24.28 ~ -23.66	16.16 ~ 16.41	3.15 ~ 3.19	16.61	-11.697
	1.65	-24.28 ~ -23.89	16.65 ~ 16.89	3.01 ~ 3.05	21.21	-11.8336
FS	1.35	-25.91 ~ -30.69	16.11 ~ 16.4	3.16 ~ 3.21	12.32	-12.2115
	1.5	-29.09 ~ -32.0	17.18 ~ 17.42	2.67 ~ 2.71	16.33	-12.7438
	1.65	-28.41 ~ -31.54	17.64 ~ 17.86	2.55 ~ 2.59	20.9	-12.863
SF	1.35	-25.92 ~ -30.68	16.11 ~ 16.4	3.16 ~ 3.21	12.32	-12.2115
	1.5	-29.1 ~ -32.0	17.18 ~ 17.42	2.67 ~ 2.71	16.33	-12.7438
	1.65	-28.42 ~ -31.54	17.64 ~ 17.86	2.55 ~ 2.59	20.9	-12.863

3.3~3.4 GHz Post-Simulation in 5-Corner Libraries

Model Library	VDD (V)	3.3~3.4 GHz				
		S11(dB)	S21(dB)	NF(dB)	Power (mW)	IIP3(dBm)
TT	1.35	-16.74 ~ -12.67	15.12 ~ 15.47	2.57 ~ 2.59	8.842	-12.1567
	1.5	-16.82 ~ -12.94	15.5 ~ 15.88	2.52 ~ 2.54	11.75	-12.2675
	1.65	-16.65 ~ -13.13	15.79 ~ 16.18	2.49 ~ 2.51	15.609	-12.3331
FF	1.35	-16.07 ~ -12.3	15.6 ~ 15.96	2.34 ~ 2.35	8.73	-12.8336
	1.5	-15.81 ~ -12.41	15.97 ~ 16.35	2.29 ~ 2.31	11.64	-12.8186
	1.65	-15.46 ~ -12.46	16.24 ~ 16.64	2.26 ~ 2.2)	14.95	-12.9336
SS	1.35	-17.23 ~ -13.02	14.27 ~ 14.62	3.01 ~ 3.03	9.01	-11.5476
	1.5	-17.96 ~ -13.56	14.68 ~ 15.05	2.95 ~ 2.97	11.94	-11.6407
	1.65	-18.39 ~ -14.0	14.99 ~ 15.38	2.90 ~ 2.92	15.28	-11.5671
FS	1.35	-16.71 ~ -12.67	15.21 ~ 15.47	2.57 ~ 2.59	8.84	-12.1567
	1.5	-16.82 ~ -12.94	15.5 ~ 15.88	2.52 ~ 2.54	11.76	-12.2675
	1.65	-16.65 ~ -13.13	15.79 ~ 16.18	2.49 ~ 2.51	15.09	-12.3331
SF	1.35	-16.47 ~ -12.67	15.12 ~ 15.47	2.57 ~ 2.59	8.84	-12.1567
	1.5	-16.82 ~ -12.94	15.5 ~ 15.88	2.52 ~ 2.54	11.76	-12.2675
	1.65	-16.65 ~ -13.13	15.79 ~ 16.18	2.49 ~ 2.51	15.09	-12.3331