LAMPIRAN

LAMPIRAN 1

Data Sheet *microcontroller* AVR Tipe ATmega16

Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 16K Bytes of In-System Self-Programmable Flash
    Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - 512 Bytes EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 1K Byte Internal SRAM
  - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 8-channel, 10-bit ADC
    8 Single-ended Channels
    7 Differential Channels in TQFP Package Only
    2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega16L
  - 4.5 - 5.5V for ATmega16
- Speed Grades
  - 0 - 8 MHz for ATmega16L
  - 0 - 16 MHz for ATmega16
- Power Consumption @ 1 MHz, 3V, and 25°C for ATmega16L
  - Active: 1.1 mA
  - Idle Mode: 0.35 mA
  - Power-down Mode: < 1 µA

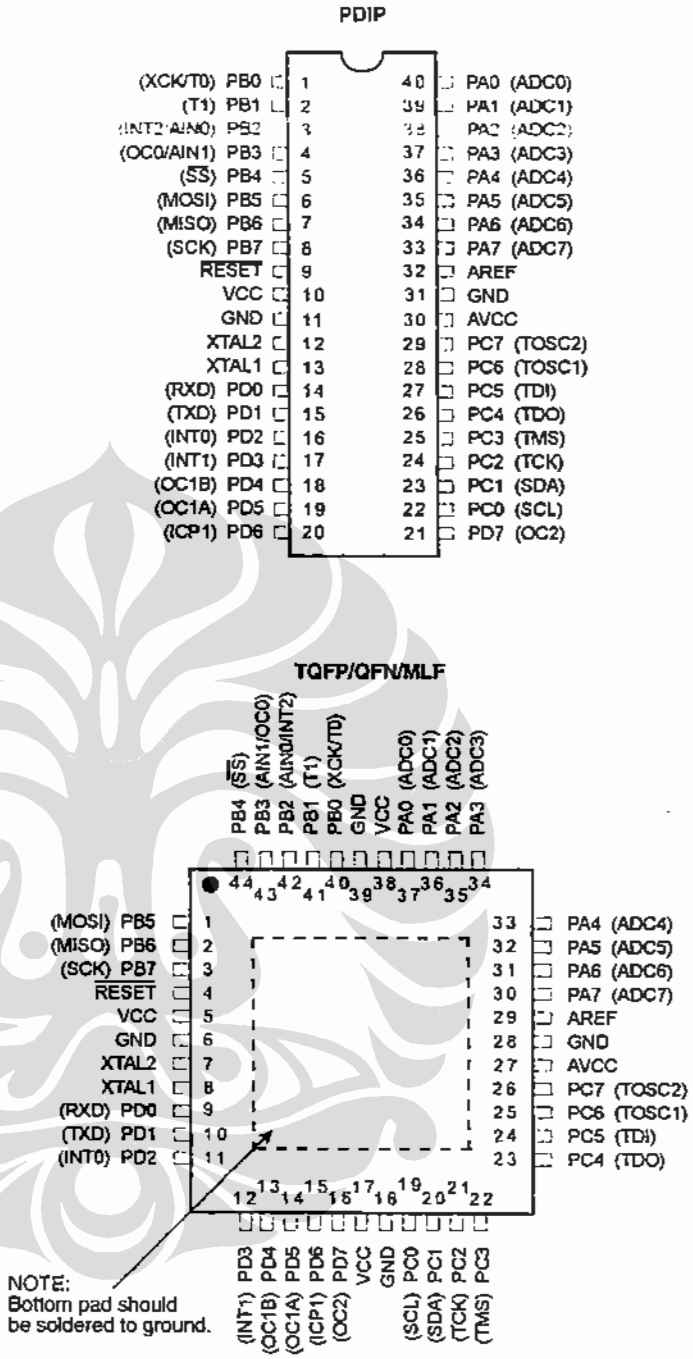
8-bit AVR® Microcontroller with 16K Bytes In-System Programmable Flash

ATmega16
ATmega16L

2466O–AVR–03/07

Pin Configurations

Figure 1. Pinout ATmega16



Disclaimer

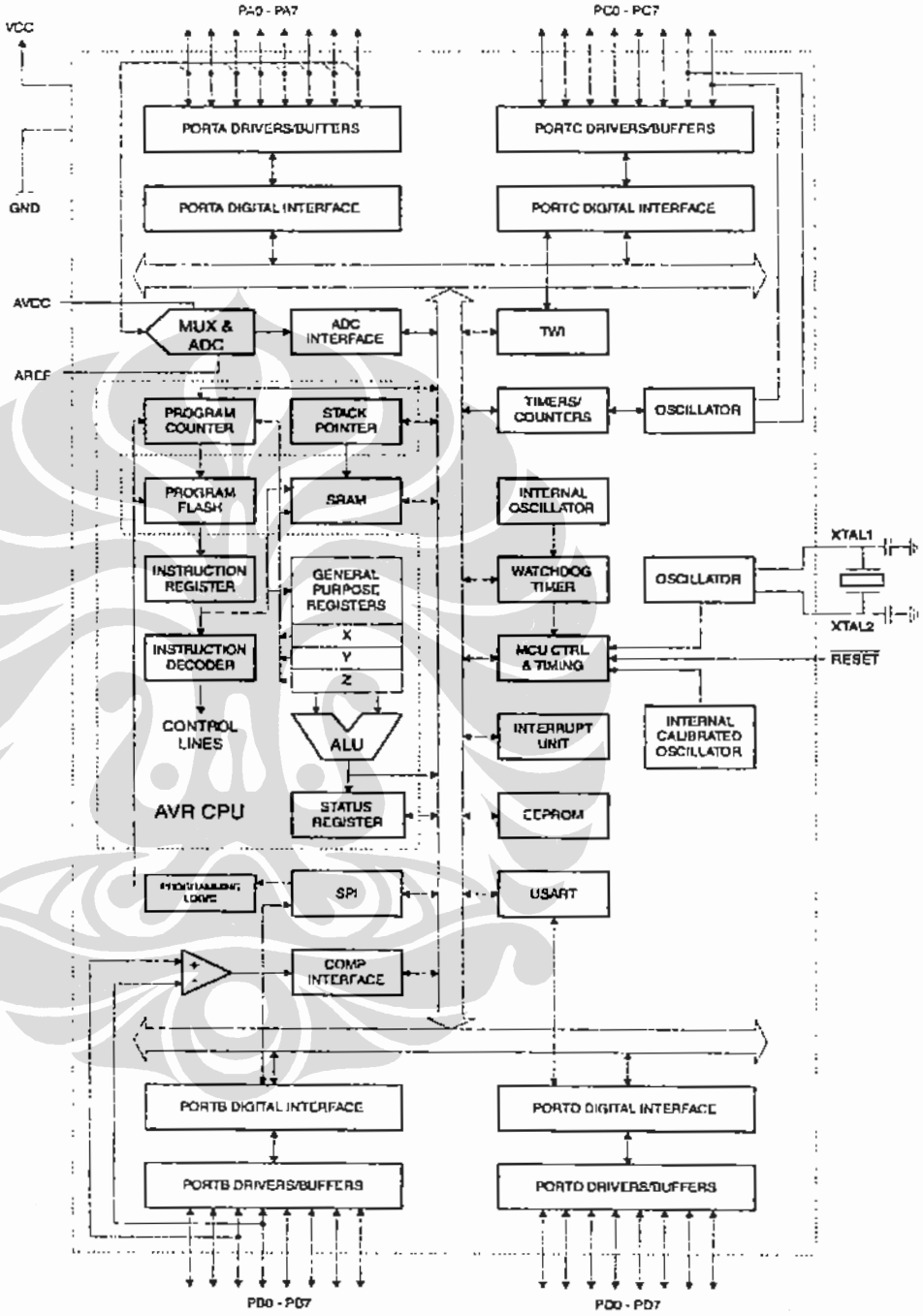
Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

Overview

The ATmega16 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega16 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 2. Block Diagram



LAMPIRAN 2

Data Sheet *Optoisolator* 4N25/26

GlobalOptoisolator™

VDE UL CSA SETI SEMKO DEMKO NEMKO BART

6-Pin DIP Optoisolators Transistor Output

4N25*
4N25A*
4N26*
(CTR = 20% Min)
4N27
4N28
(CTR = 10% Min)

*Motorola Preferred Devices

The 4N25/A, 4N26, 4N27 and 4N28 devices consist of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon phototransistor detector.

- Most Economical Optoisolator Choice for Medium Speed, Switching Applications
- Meets or Exceeds All JEDEC Registered Specifications
- ***To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.***

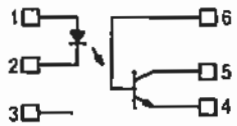
Applications

- General Purpose Switching Circuits
- Interfacing and coupling systems of different potentials and impedances
- I/O Interfacing
- Solid State Relays

STYLE 1 PLASTIC

STANDARD THRU HOLE
CASE 730A–04

SCHEMATIC



PIN 1. LED ANODE
2. LED CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT LED			
Reverse Voltage	V_R	3	Volts
Forward Current — Continuous	I_F	60	mA
LED Power Dissipation @ T_A = 25°C with Negligible Power in Output Detector	P_D	120	mW
Derate above 25°C		1.41	mW/°C
OUTPUT TRANSISTOR			
Collector–Emitter Voltage	V_{CEO}	30	Volts
Emitter–Collector Voltage	V_{ECO}	7	Volts
Collector–Base Voltage	V_{CBO}	70	Volts
Collector Current — Continuous	I_C	150	mA
Detector Power Dissipation @ T_A = 25°C with Negligible Power in Input LED	P_D	150	mW
Derate above 25°C		1.76	mW/°C
TOTAL DEVICE			
Isolation Surge Voltage(1) (Peak ac Voltage, 60 Hz, 1 sec Duration)	V_{ISO}	7500	Vac(pk)
Total Device Power Dissipation @ T_A = 25°C	P_D	250	mW
Derate above 25°C		2.94	mW/°C
Ambient Operating Temperature Range(2)	T_A	−55 to +100	°C
Storage Temperature Range(2)	T_{stg}	−55 to +150	°C
Soldering Temperature (10 sec, 1/16" from case)	T_L	260	°C

1. Isolation surge voltage is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.
2. Refer to Quality and Reliability Section in Opto Data Book for information on test conditions.

Preferred devices are Motorola recommended choices for future use and best overall value.

GlobalOptoisolator is a trademark of Motorola, Inc.

REV 5

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ(1)	Max	Unit
INPUT LED						
Forward Voltage (I_F = 10 mA)	T_A = 25°C T_A = –55°C T_A = 100°C	V_F	— — —	1.15 1.3 1.05	1.5 — —	Volts
Reverse Leakage Current (V_R = 3 V)		I_R	—	—	100	µA
Capacitance (V = 0 V, f = 1 MHz)		C_J	—	18	—	pF
OUTPUT TRANSISTOR						
Collector–Emitter Dark Current (V_{CE} = 10 V, T_A = 25°C	4N25,25A,26,27 4N28	I_{CEO}	— —	1 1	50 100	nA
(V_{CE} = 10 V, T_A = 100°C)	All Devices	I_{CEO}	—	1	—	µA
Collector–Base Dark Current (V_{CB} = 10 V)		I_{CBO}	—	0.2	—	nA
Collector–Emitter Breakdown Voltage (I_C = 1 mA)		$V_{(BR)CEO}$	30	45	—	Volts
Collector–Base Breakdown Voltage (I_C = 100 µA)		$V_{(BR)CBO}$	70	100	—	Volts
Emitter–Collector Breakdown Voltage (I_E = 100 µA)		$V_{(BR)ECO}$	7	7.8	—	Volts
DC Current Gain (I_C = 2 mA, V_{CE} = 5 V)		h_{FE}	—	500	—	—
Collector–Emitter Capacitance (f = 1 MHz, V_{CE} = 0)		C_{CE}	—	7	—	pF
Collector–Base Capacitance (f = 1 MHz, V_{CB} = 0)		C_{CB}	—	19	—	pF
Emitter–Base Capacitance (f = 1 MHz, V_{EB} = 0)		C_{EB}	—	9	—	pF
COUPLED						
Output Collector Current (I_F = 10 mA, V_{CE} = 10 V)	4N25,25A,26 4N27,28	I_C (CTR)(2)	2 (20) 1 (10)	7 (70) 5 (50)	— —	mA (%)
Collector–Emitter Saturation Voltage (I_C = 2 mA, I_F = 50 mA)		$V_{CE(sat)}$	—	0.15	0.5	Volts
Turn–On Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_{on}	—	2.8	—	µs
Turn–Off Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_{off}	—	4.5	—	µs
Rise Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_r	—	1.2	—	µs
Fall Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_f	—	1.3	—	µs
Isolation Voltage (f = 60 Hz, t = 1 sec)(4)		V_{ISO}	7500	—	—	Vac(pk)
Isolation Resistance (V = 500 V)(4)		R_{ISO}	10^{11}	—	—	Ω
Isolation Capacitance (V = 0 V, f = 1 MHz)(4)		C_{ISO}	—	0.2	—	pF

1. Always design to the specified minimum/maximum electrical limits (where applicable).
2. Current Transfer Ratio (CTR) = I_C/I_F x 100%.
3. For test circuit setup and waveforms, refer to Figure 11.
4. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

LAMPIRAN 3

Data Sheet Transistor daya BJT 2SD2553

TOSHIBA TRANSISTOR SILICON NPN TRIPLE DIFFUSED MESA TYPE

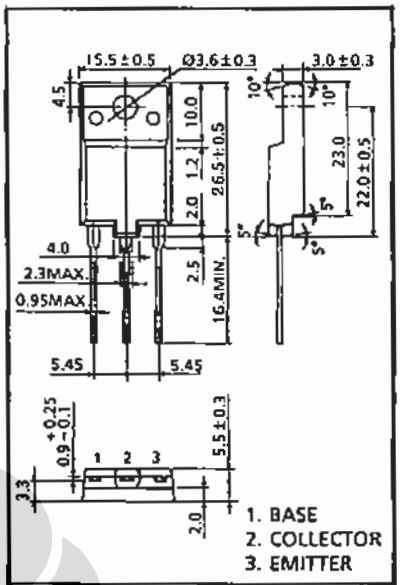
2SD2553

HORIZONTAL DEFLECTION OUTPUT FOR HIGH RESOLUTION DISPLAY, COLOR TV

HIGH SPEED SWITCHING APPLICATIONS

- High Voltage : V_{CBO} = 1700 V
- Low Saturation Voltage : $V_{CE\ (sat)}$ = 5 V (Max.)
- High Speed : t_f = 0.3 μs (Typ.)
- Bult-in Damper Type
- Collector Metal (Fin) is Fully Covered with Mold Resin.

Unit in mm



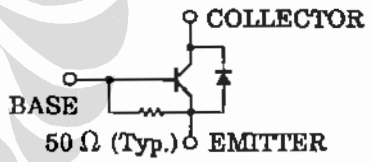
JEDEC	—
EIAJ	—
TOSHIBA	2-16E3A

Weight : 5.5 g (Typ.)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector-Base Voltage		V_{CBO}	1700	V
Collector-Emitter Voltage		V_{CEO}	600	V
Emitter-Base Voltage		V_{EBO}	5	V
Collector Current	DC	I_C	8	A
	Pulse	I_{CP}	16	
Base Current		I_B	4	A
Collector Power Dissipation (Tc = 25°C)		P_C	50	W
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	−55~150	°C

EQUIVALENT CIRCUIT

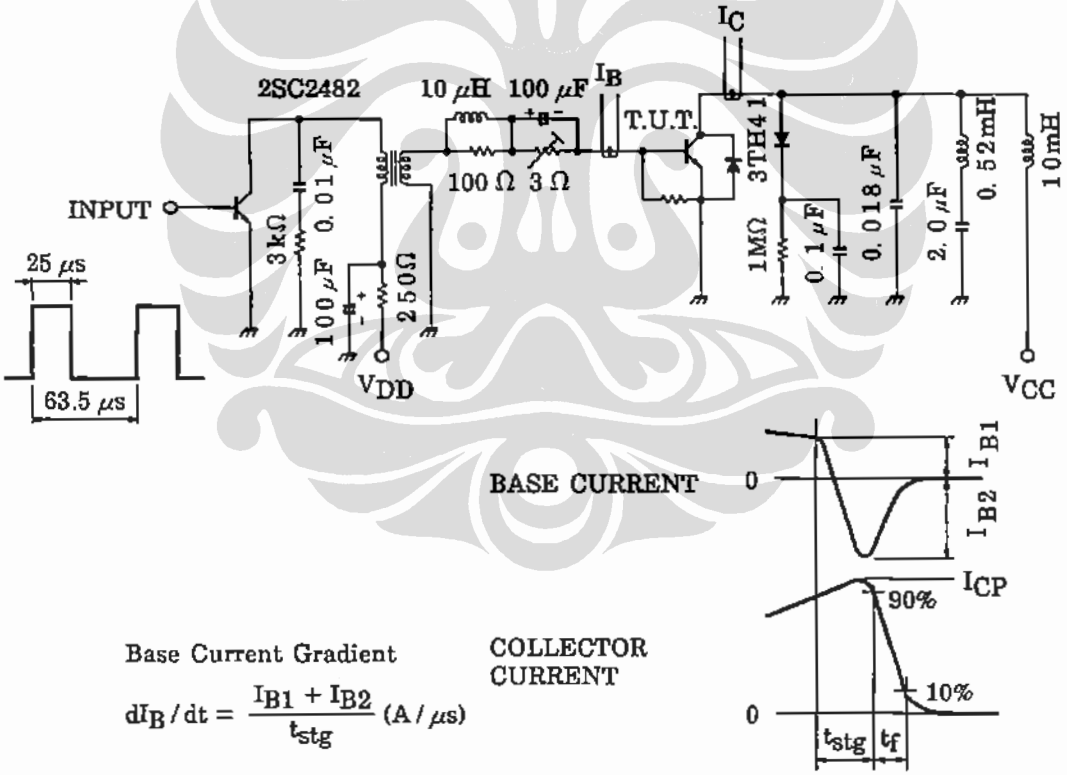


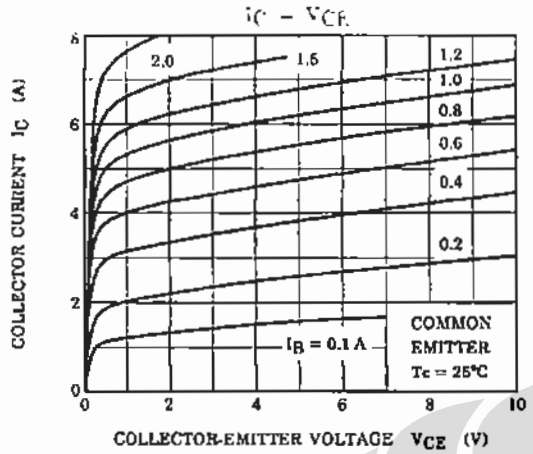
961001EAA1

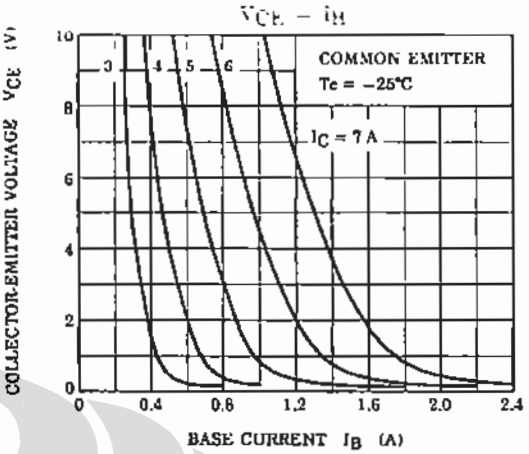
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

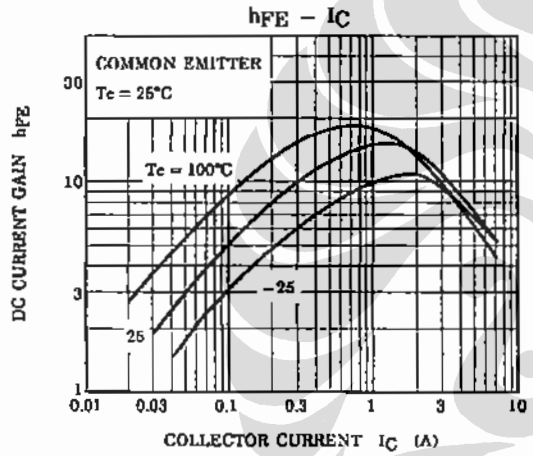
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current		I_{CBO}	V_{CB} = 1700 V, I_E = 0	—	—	1	mA
Emitter Cut-off Current		I_{EBO}	V_{EB} = 5 V, I_C = 0	66	—	200	mA
Emitter-Base Breakdown Voltage		V_{EBO}	I_E = 400 mA, I_C = 0	5	—	—	V
DC Current Gain		$h_{FE(1)}$	V_{CE} = 5 V, I_C = 1 A	8	—	28	—
		$h_{FE(2)}$	V_{CE} = 5 V, I_C = 6 A	5	—	9	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	I_C = 6 A, I_B = 1.2 A	—	—	5	V
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	I_C = 6 A, I_B = 1.2 A	—	0.9	1.2	V
Forward Voltage (Damper Diode)		$-V_F$	I_F = 8 A	—	1.6	2.0	V
Transition Frequency		f_T	V_{CE} = 10 V, I_C = 0.1 A	—	2	—	MHz
Collector Output Capacitance		C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1 MHz	—	155	—	pF
Switching Time (Fig.1)	Storage Time	t_{stg}	I_{CP} = 6 A, $I_{B1(end)}$ = 1.5 A	—	9	12	μs
	Fall Time	t_f	f_H = 15.75 kHz	—	0.3	0.7	

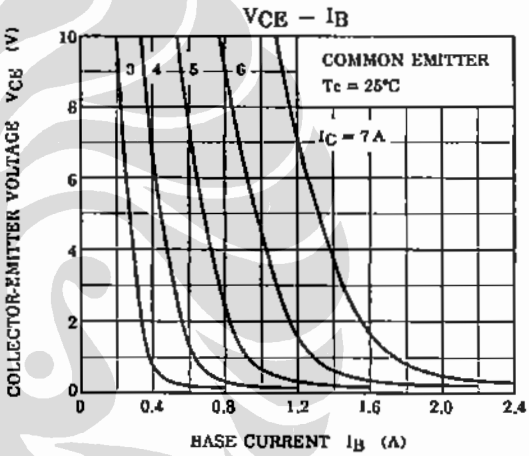
Fig.1 Switching time test circuit

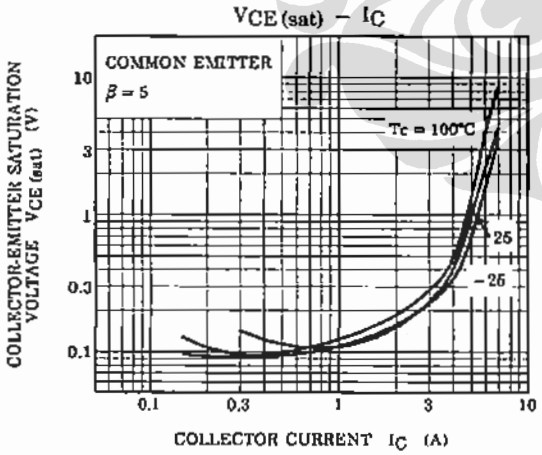


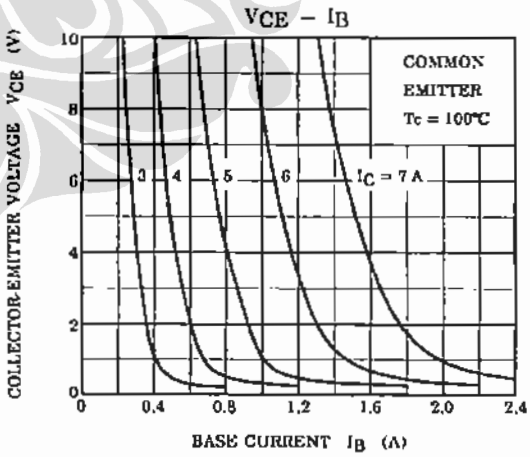

COLLECTOR CURRENT I_C (A)
2.0
1.5
1.2
1.0
0.8
0.6
0.4
0.2
I_B = 0.1 A
COMMON EMITTER
Tc = 25°C
COLLECTOR-EMITTER VOLTAGE V_{CE} (V)


COLLECTOR-EMITTER VOLTAGE V_{CE} (V)
COMMON EMITTER
Tc = −25°C
I_C = 7 A
BASE CURRENT I_B (A)

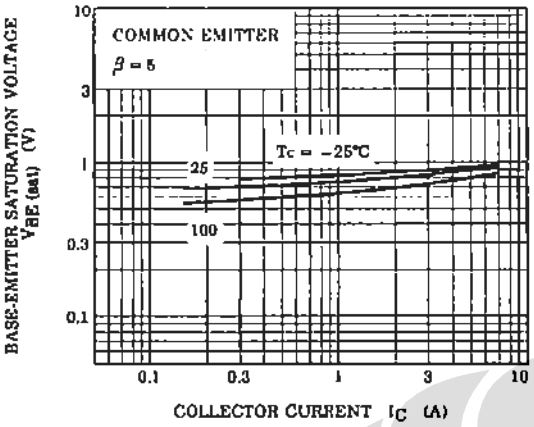

h_{FE} – I_C
DC CURRENT GAIN h_{FE}
COMMON EMITTER
Tc = 25°C
Tc = 100°C
−25
25
COLLECTOR CURRENT I_C (A)


V_{CE} – I_B
COLLECTOR-EMITTER VOLTAGE V_{CE} (V)
COMMON EMITTER
Tc = 25°C
I_C = 7 A
BASE CURRENT I_B (A)

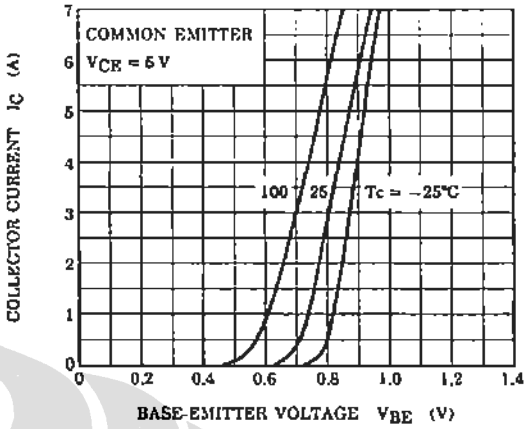

$V_{CE(sat)}$ – I_C
COLLECTOR-EMITTER SATURATION VOLTAGE $V_{CE(sat)}$ (V)
COMMON EMITTER
β = 5
Tc = 100°C
25
−25
COLLECTOR CURRENT I_C (A)


V_{CE} – I_B
COLLECTOR-EMITTER VOLTAGE V_{CE} (V)
COMMON EMITTER
Tc = 100°C
I_C = 7 A
BASE CURRENT I_B (A)

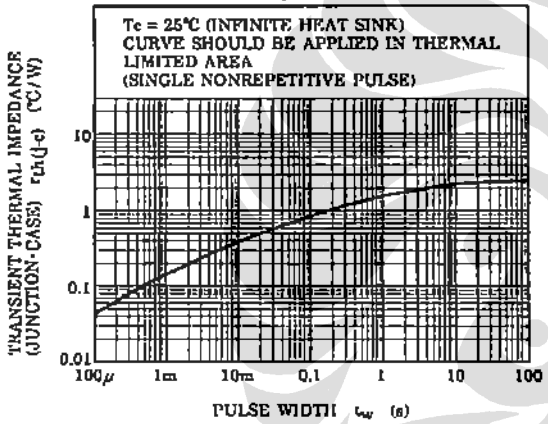
$V_{BE(sat)}$ – I_C



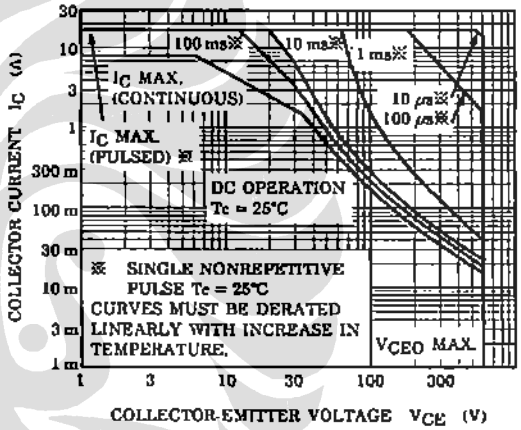
I_C – V_{BE}



$r_{th(j-c)}$ – t_w



SAFE OPERATING AREA



P_C – Tc